

## Features

- High Performance, Low Power AVR<sup>®</sup>32 UC 32-Bit Microcontroller
  - Compact Single-cycle RISC Instruction Set Including DSP Instruction Set
  - Read-Modify-Write Instructions and Atomic Bit Manipulation
  - Performing 1.38 DMIPS / MHz
    - Up to 83 DMIPS Running at 66 MHz from Flash (1 Wait-State)
    - Up to 45 DMIPS Running at 33MHz from Flash (0 Wait-State)
  - Memory Protection Unit
- Multi-hierarchy Bus System
  - High-Performance Data Transfers on Separate Buses for Increased Performance
  - 15 Peripheral DMA Channels Improves Speed for Peripheral Communication
- Internal High-Speed Flash
  - 512K Bytes, 256K Bytes, 128K Bytes Versions
  - Single Cycle Access up to 33 MHz
  - Prefetch Buffer Optimizing Instruction Execution at Maximum Speed
  - 4ms Page Programming Time and 8ms Full-Chip Erase Time
  - 100,000 Write Cycles, 15-year Data Retention Capability
  - Flash Security Locks and User Defined Configuration Area
- Internal High-Speed SRAM, Single-Cycle Access at Full Speed
  - 64K Bytes (512KB and 256KB Flash), 32K Bytes (128KB Flash)
- External Memory Interface on AT32UC3A0 Derivatives
  - SDRAM / SRAM Compatible Memory Bus (16-bit Data and 24-bit Address Buses)
- Interrupt Controller
  - Autovector Low Latency Interrupt Service with Programmable Priority
- System Functions
  - Power and Clock Manager Including Internal RC Clock and One 32KHz Oscillator
  - Two Multipurpose Oscillators and Two Phase-Lock-Loop (PLL) allowing Independent CPU Frequency from USB Frequency
  - Watchdog Timer, Real-Time Clock Timer
- Universal Serial Bus (USB)
  - Device 2.0 Full Speed and On-The-Go (OTG) Low Speed and Full Speed
  - Flexible End-Point Configuration and Management with Dedicated DMA Channels
  - On-chip Transceivers Including Pull-Ups
- Ethernet MAC 10/100 Mbps interface
  - 802.3 Ethernet Media Access Controller
  - Supports Media Independent Interface (MII) and Reduced MII (RMII)
- One Three-Channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, PWM, Capture and Various Counting Capabilities
- One 7-Channel 16-bit Pulse Width Modulation Controller (PWM)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - Independent Baudrate Generator, Support for SPI, IrDA and ISO7816 interfaces
  - Support for Hardware Handshaking, RS485 Interfaces and Modem Line
- Two Master/Slave Serial Peripheral Interfaces (SPI) with Chip Select Signals
- One Synchronous Serial Protocol Controller
  - Supports I2S and Generic Frame-Based Protocols
- One Master/Slave Two-Wire Interface (TWI), 400kbit/s I2C-compatible
- One 8-channel 10-bit Analog-To-Digital Converter
- 16-bit Stereo Audio Bitstream
  - Sample Rate Up to 50 KHz



## AVR<sup>®</sup>32 32-Bit Microcontroller

AT32UC3A0512  
AT32UC3A0256  
AT32UC3A0128  
AT32UC3A1512  
AT32UC3A1256  
AT32UC3A1128

## Preliminary

## Summary

32058ES-AVR32-04/08



- On-Chip Debug System (JTAG interface)
  - Nexus Class 2+, Runtime Control, Non-Intrusive Data and Program Trace
- 100-pin TQFP (69 GPIO pins), 144-pin LQFP (109 GPIO pins)
- 5V Input Tolerant I/Os
- Single 3.3V Power Supply or Dual 1.8V-3.3V Power Supply

# KTTIC

## 1. Description

The AT32UC3A is a complete System-On-Chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 66 MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems. Higher computation capabilities are achievable using a rich set of DSP instructions.

The AT32UC3A incorporates on-chip Flash and SRAM memories for secure and fast access. For applications requiring additional memory, an external memory interface is provided on AT32UC3A0 derivatives.

The Peripheral Direct Memory Access controller (PDCA) enables data transfers between peripherals and memories without processor involvement. PDCA drastically reduces processing overhead when transferring continuous and large data streams between modules within the MCU.

The PowerManager improves design flexibility and security: the on-chip Brown-Out Detector monitors the power supply, the CPU runs from the on-chip RC oscillator or from one of external oscillator sources, a Real-Time Clock and its associated timer keeps track of the time.

The Timer/Counter includes three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

The PWM modules provides seven independent channels with many configuration options including polarity, edge alignment and waveform non overlap control. One PWM channel can trigger ADC conversions for more accurate close loop control implementations.

The AT32UC3A also features many communication interfaces for communication intensive applications. In addition to standard serial interfaces like UART, SPI or TWI, other interfaces like flexible Synchronous Serial Controller, USB and Ethernet MAC are available.

The Synchronous Serial Controller provides easy access to serial communication protocols and audio standards like I2S.

The Full-Speed USB 2.0 Device interface supports several USB Classes at the same time thanks to the rich End-Point configuration. The On-The-GO (OTG) Host interface allows device like a USB Flash disk or a USB printer to be directly connected to the processor.

The media-independent interface (MII) and reduced MII (RMII) 10/100 Ethernet MAC module provides on-chip solutions for network-connected devices.

AT32UC3A integrates a class 2+ Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control.

## 2. Configuration Summary

The table below lists all AT32UC3A memory and package configurations:

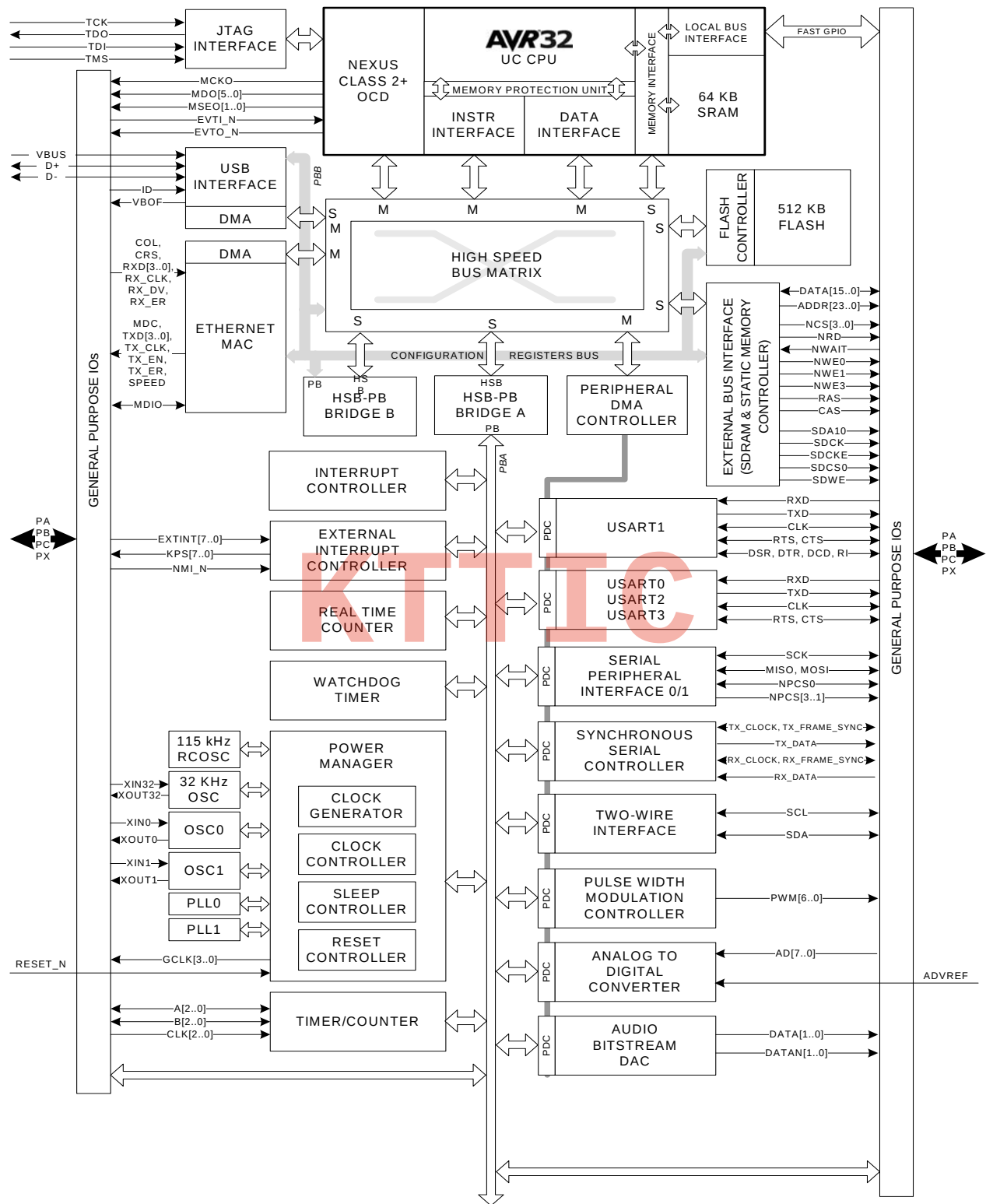
| Device       | Flash      | SRAM      | Ext. Bus Interface | Ethernet MAC | Package       |
|--------------|------------|-----------|--------------------|--------------|---------------|
| AT32UC3A0512 | 512 Kbytes | 64 Kbytes | yes                | yes          | 144 lead LQFP |
| AT32UC3A0256 | 256 Kbytes | 64 Kbytes | yes                | yes          | 144 lead LQFP |
| AT32UC3A0128 | 128 Kbytes | 32 Kbytes | yes                | yes          | 144 lead LQFP |
| AT32UC3A1512 | 512 Kbytes | 64 Kbytes | no                 | yes          | 100 lead TQFP |
| AT32UC3A1256 | 256 Kbytes | 64 Kbytes | no                 | yes          | 100 lead TQFP |
| AT32UC3A1128 | 128 Kbytes | 32 Kbytes | no                 | yes          | 100 lead TQFP |

## 3. Abbreviations

- GCLK: Power Manager Generic Clock
- GPIO: General Purpose Input/Output
- HSB: High Speed Bus
- MPU: Memory Protection Unit
- OCD: On Chip Debug
- PB: Peripheral Bus
- PDCA: Peripheral Direct Memory Access Controller (PDC) version A
- USBB: USB On-The-GO Controller version B

4. Blockdiagram

Figure 4-1. Blockdiagram



## 4.1 Processor and architecture

### 4.1.1 AVR32 UC CPU

- 32-bit load/store AVR32A RISC architecture.
  - 15 general-purpose 32-bit registers.
  - 32-bit Stack Pointer, Program Counter and Link Register reside in register file.
  - Fully orthogonal instruction set.
  - Privileged and unprivileged modes enabling efficient and secure Operating Systems.
  - Innovative instruction set together with variable instruction length ensuring industry leading code density.
  - DSP extension with saturating arithmetic, and a wide variety of multiply instructions.
- 3 stage pipeline allows one instruction per clock cycle for most instructions.
  - Byte, half-word, word and double word memory access.
  - Multiple interrupt priority levels.
- MPU allows for operating systems with memory protection.

### 4.1.2 Debug and Test system

- IEEE1149.1 compliant JTAG and boundary scan
- Direct memory access and programming capabilities through JTAG interface
- Extensive On-Chip Debug features in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 2+
  - Low-cost NanoTrace supported.
- Auxiliary port for high-speed trace information
- Hardware support for 6 Program and 2 data breakpoints
- Unlimited number of software breakpoints supported
- Advanced Program, Data, Ownership, and Watchpoint trace supported

### 4.1.3 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Fifteen channels
  - Two for each USART
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - One for each ADC
  - Two for each TWI Interface

### 4.1.4 Bus system

- High Speed Bus (HSB) matrix with 6 Masters and 6 Slaves handled
  - Handles Requests from the CPU Data Fetch, CPU Instruction Fetch, PDCA, USBB, Ethernet Controller, CPU SAB, and to internal Flash, internal SRAM, Peripheral Bus A, Peripheral Bus B, EBI.
  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst Breaking with Slot Cycle Limit
  - One Address Decoder Provided per Master

- Peripheral Bus A able to run on at divided bus speeds compared to the High Speed Bus

Figure 4-1 gives an overview of the bus system. All modules connected to the same bus use the same clock, but the clock to each module can be individually shut off by the Power Manager. The figure identifies the number of master and slave interfaces of each module connected to the High Speed Bus, and which DMA controller is connected to which peripheral.

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## 5. Signals Description

The following table gives details on the signal name classified by peripheral

The signals are multiplexed with GPIO pins as described in "[Peripheral Multiplexing on I/O lines](#)" on page 30.

**Table 5-1.** Signal Description List

| Signal Name                           | Function                       | Type         | Active Level | Comments        |
|---------------------------------------|--------------------------------|--------------|--------------|-----------------|
| <b>Power</b>                          |                                |              |              |                 |
| VDDPLL                                | Power supply for PLL           | Power Input  |              | 1.65V to 1.95 V |
| VDDCORE                               | Core Power Supply              | Power Input  |              | 1.65V to 1.95 V |
| VDDIO                                 | I/O Power Supply               | Power Input  |              | 3.0V to 3.6V    |
| VDDANA                                | Analog Power Supply            | Power Input  |              | 3.0V to 3.6V    |
| VDDIN                                 | Voltage Regulator Input Supply | Power Input  |              | 3.0V to 3.6V    |
| VDDOUT                                | Voltage Regulator Output       | Power Output |              | 1.65V to 1.95 V |
| GNDANA                                | Analog Ground                  | Ground       |              |                 |
| GND                                   | Ground                         | Ground       |              |                 |
| <b>Clocks, Oscillators, and PLL's</b> |                                |              |              |                 |
| XIN0, XIN1, XIN32                     | Crystal 0, 1, 32 Input         | Analog       |              |                 |
| XOUT0, XOUT1, XOUT32                  | Crystal 0, 1, 32 Output        | Analog       |              |                 |
| <b>JTAG</b>                           |                                |              |              |                 |
| TCK                                   | Test Clock                     | Input        |              |                 |
| TDI                                   | Test Data In                   | Input        |              |                 |
| TDO                                   | Test Data Out                  | Output       |              |                 |
| TMS                                   | Test Mode Select               | Input        |              |                 |
| <b>Auxiliary Port - AUX</b>           |                                |              |              |                 |
| MCKO                                  | Trace Data Output Clock        | Output       |              |                 |
| MDO0 - MDO5                           | Trace Data Output              | Output       |              |                 |



**Table 5-1.** Signal Description List

| Signal Name                                | Function                          | Type   | Active Level | Comments |
|--------------------------------------------|-----------------------------------|--------|--------------|----------|
| MSEO0 - MSEO1                              | Trace Frame Control               | Output |              |          |
| EVTI_N                                     | Event In                          | Output | Low          |          |
| EVTO_N                                     | Event Out                         | Output | Low          |          |
| <b>Power Manager - PM</b>                  |                                   |        |              |          |
| GCLK0 - GCLK3                              | Generic Clock Pins                | Output |              |          |
| RESET_N                                    | Reset Pin                         | Input  | Low          |          |
| <b>Real Time Counter - RTC</b>             |                                   |        |              |          |
| RTC_CLOCK                                  | RTC clock                         | Output |              |          |
| <b>Watchdog Timer - WDT</b>                |                                   |        |              |          |
| WDTEXT                                     | External Watchdog Pin             | Output |              |          |
| <b>External Interrupt Controller - EIC</b> |                                   |        |              |          |
| EXTINT0 - EXTINT7                          | External Interrupt Pins           | Input  |              |          |
| KPS0 - KPS7                                | Keypad Scan Pins                  | Output |              |          |
| NMI_N                                      | Non-Maskable Interrupt Pin        | Input  | Low          |          |
| <b>Ethernet MAC - MACB</b>                 |                                   |        |              |          |
| COL                                        | Collision Detect                  | Input  |              |          |
| CRS                                        | Carrier Sense and Data Valid      | Input  |              |          |
| MDC                                        | Management Data Clock             | Output |              |          |
| MDIO                                       | Management Data Input/Output      | I/O    |              |          |
| RXD0 - RXD3                                | Receive Data                      | Input  |              |          |
| RX_CLK                                     | Receive Clock                     | Input  |              |          |
| RX_DV                                      | Receive Data Valid                | Input  |              |          |
| RX_ER                                      | Receive Coding Error              | Input  |              |          |
| SPEED                                      | Speed                             |        |              |          |
| TXD0 - TXD3                                | Transmit Data                     | Output |              |          |
| TX_CLK                                     | Transmit Clock or Reference Clock | Output |              |          |
| TX_EN                                      | Transmit Enable                   | Output |              |          |
| TX_ER                                      | Transmit Coding Error             | Output |              |          |

Table 5-1. Signal Description List

| Signal Name                                                 | Function                      | Type   | Active Level | Comments |
|-------------------------------------------------------------|-------------------------------|--------|--------------|----------|
| <b>External Bus Interface - HEBI</b>                        |                               |        |              |          |
| ADDR0 - ADDR23                                              | Address Bus                   | Output |              |          |
| CAS                                                         | Column Signal                 | Output | Low          |          |
| DATA0 - DATA15                                              | Data Bus                      | I/O    |              |          |
| NCS0 - NCS3                                                 | Chip Select                   | Output | Low          |          |
| NRD                                                         | Read Signal                   | Output | Low          |          |
| NWAIT                                                       | External Wait Signal          | Input  | Low          |          |
| NWE0                                                        | Write Enable 0                | Output | Low          |          |
| NWE1                                                        | Write Enable 1                | Output | Low          |          |
| NWE3                                                        | Write Enable 3                | Output | Low          |          |
| RAS                                                         | Row Signal                    | Output | Low          |          |
| SDA10                                                       | SDRAM Address 10 Line         | Output |              |          |
| SDCK                                                        | SDRAM Clock                   | Output |              |          |
| SDCKE                                                       | SDRAM Clock Enable            | Output |              |          |
| SDCS0                                                       | SDRAM Chip Select             | Output | Low          |          |
| SDWE                                                        | SDRAM Write Enable            | Output | Low          |          |
| <b>General Purpose Input/Output 2 - GPIOA, GPIOB, GPIOC</b> |                               |        |              |          |
| P0 - P31                                                    | Parallel I/O Controller GPIOA | I/O    |              |          |
| P0 - P31                                                    | Parallel I/O Controller GPIOB | I/O    |              |          |
| P0 - P5                                                     | Parallel I/O Controller GPIOC | I/O    |              |          |
| P0 - P31                                                    | Parallel I/O Controller GPIOX | I/O    |              |          |
| <b>Serial Peripheral Interface - SPI0, SPI1</b>             |                               |        |              |          |
| MISO                                                        | Master In Slave Out           | I/O    |              |          |
| MOSI                                                        | Master Out Slave In           | I/O    |              |          |
| NPCS0 - NPCS3                                               | SPI Peripheral Chip Select    | I/O    | Low          |          |
| SCK                                                         | Clock                         | Output |              |          |
| <b>Synchronous Serial Controller - SSC</b>                  |                               |        |              |          |
| RX_CLOCK                                                    | SSC Receive Clock             | I/O    |              |          |

**Table 5-1.** Signal Description List

| Signal Name                                                                                     | Function                       | Type   | Active Level | Comments    |
|-------------------------------------------------------------------------------------------------|--------------------------------|--------|--------------|-------------|
| RX_DATA                                                                                         | SSC Receive Data               | Input  |              |             |
| RX_FRAME_SYNC                                                                                   | SSC Receive Frame Sync         | I/O    |              |             |
| TX_CLOCK                                                                                        | SSC Transmit Clock             | I/O    |              |             |
| TX_DATA                                                                                         | SSC Transmit Data              | Output |              |             |
| TX_FRAME_SYNC                                                                                   | SSC Transmit Frame Sync        | I/O    |              |             |
| <b>Timer/Counter - TIMER</b>                                                                    |                                |        |              |             |
| A0                                                                                              | Channel 0 Line A               | I/O    |              |             |
| A1                                                                                              | Channel 1 Line A               | I/O    |              |             |
| A2                                                                                              | Channel 2 Line A               | I/O    |              |             |
| B0                                                                                              | Channel 0 Line B               | I/O    |              |             |
| B1                                                                                              | Channel 1 Line B               | I/O    |              |             |
| B2                                                                                              | Channel 2 Line B               | I/O    |              |             |
| CLK0                                                                                            | Channel 0 External Clock Input | Input  |              |             |
| CLK1                                                                                            | Channel 1 External Clock Input | Input  |              |             |
| CLK2                                                                                            | Channel 2 External Clock Input | Input  |              |             |
| <b>Two-wire Interface - TWI</b>                                                                 |                                |        |              |             |
| SCL                                                                                             | Serial Clock                   | I/O    |              |             |
| SDA                                                                                             | Serial Data                    | I/O    |              |             |
| <b>Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3</b> |                                |        |              |             |
| CLK                                                                                             | Clock                          | I/O    |              |             |
| CTS                                                                                             | Clear To Send                  | Input  |              |             |
| DCD                                                                                             | Data Carrier Detect            |        |              | Only USART1 |
| DSR                                                                                             | Data Set Ready                 |        |              | Only USART1 |
| DTR                                                                                             | Data Terminal Ready            |        |              | Only USART1 |
| RI                                                                                              | Ring Indicator                 |        |              | Only USART1 |
| RTS                                                                                             | Request To Send                | Output |              |             |
| RXD                                                                                             | Receive Data                   | Input  |              |             |
| TXD                                                                                             | Transmit Data                  | Output |              |             |

**Table 5-1.** Signal Description List

| Signal Name                              | Function                                | Type         | Active Level | Comments    |
|------------------------------------------|-----------------------------------------|--------------|--------------|-------------|
| <b>Analog to Digital Converter - ADC</b> |                                         |              |              |             |
| AD0 - AD7                                | Analog input pins                       | Analog input |              |             |
| ADVREF                                   | Analog positive reference voltage input | Analog input |              | 2.6 to 3.6V |
| <b>Pulse Width Modulator - PWM</b>       |                                         |              |              |             |
| PWM0 - PWM6                              | PWM Output Pins                         | Output       |              |             |
| <b>Universal Serial Bus Device - USB</b> |                                         |              |              |             |
| DDM                                      | USB Device Port Data -                  | Analog       |              |             |
| DDP                                      | USB Device Port Data +                  | Analog       |              |             |
| VBUS                                     | USB VBUS Monitor and OTG Negotiation    | Analog Input |              |             |
| USBID                                    | ID Pin of the USB Bus                   | Input        |              |             |
| USB_VBOF                                 | USB VBUS On/off: bus power control port | output       |              |             |
| <b>Audio Bitstream DAC (ABDAC)</b>       |                                         |              |              |             |
| DATA0-DATA1                              | D/A Data out                            | Output       |              |             |
| DATAN0-DATAN1                            | D/A Data inverted out                   | Output       |              |             |

6. Package and Pinout

The device pins are multiplexed with peripheral functions as described in "Peripheral Multiplexing on I/O lines" on page 30.

Figure 6-1. TQFP100 Pinout

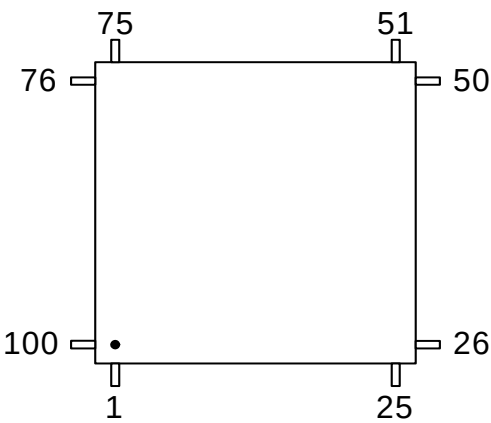


Table 6-1. TQFP100 Package Pinout

|    |         |    |         |    |        |    |         |
|----|---------|----|---------|----|--------|----|---------|
| 1  | PB20    | 26 | PA05    | 51 | PA21   | 76 | PB08    |
| 2  | PB21    | 27 | PA06    | 52 | PA22   | 77 | PB09    |
| 3  | PB22    | 28 | PA07    | 53 | PA23   | 78 | PB10    |
| 4  | VDDIO   | 29 | PA08    | 54 | PA24   | 79 | VDDIO   |
| 5  | GND     | 30 | PA09    | 55 | PA25   | 80 | GND     |
| 6  | PB23    | 31 | PA10    | 56 | PA26   | 81 | PB11    |
| 7  | PB24    | 32 | N/C     | 57 | PA27   | 82 | PB12    |
| 8  | PB25    | 33 | PA11    | 58 | PA28   | 83 | PA29    |
| 9  | PB26    | 34 | VDDCORE | 59 | VDDANA | 84 | PA30    |
| 10 | PB27    | 35 | GND     | 60 | ADVREF | 85 | PC02    |
| 11 | VDDOUT  | 36 | PA12    | 61 | GNDANA | 86 | PC03    |
| 12 | VDDIN   | 37 | PA13    | 62 | VDDPLL | 87 | PB13    |
| 13 | GND     | 38 | VDDCORE | 63 | PC00   | 88 | PB14    |
| 14 | PB28    | 39 | PA14    | 64 | PC01   | 89 | TMS     |
| 15 | PB29    | 40 | PA15    | 65 | PB00   | 90 | TCK     |
| 16 | PB30    | 41 | PA16    | 66 | PB01   | 91 | TDO     |
| 17 | PB31    | 42 | PA17    | 67 | VDDIO  | 92 | TDI     |
| 18 | RESET_N | 43 | PA18    | 68 | VDDIO  | 93 | PC04    |
| 19 | PA00    | 44 | PA19    | 69 | GND    | 94 | PC05    |
| 20 | PA01    | 45 | PA20    | 70 | PB02   | 95 | PB15    |
| 21 | GND     | 46 | VBUS    | 71 | PB03   | 96 | PB16    |
| 22 | VDDCORE | 47 | VDDIO   | 72 | PB04   | 97 | VDDCORE |

Table 6-1. TQFP100 Package Pinout

|    |      |    |     |    |      |     |      |
|----|------|----|-----|----|------|-----|------|
| 23 | PA02 | 48 | DM  | 73 | PB05 | 98  | PB17 |
| 24 | PA03 | 49 | DP  | 74 | PB06 | 99  | PB18 |
| 25 | PA04 | 50 | GND | 75 | PB07 | 100 | PB19 |

Figure 6-2. LQFP144 Pinout

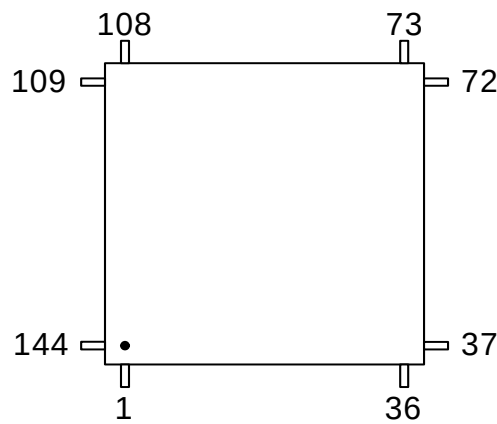


Table 6-2. VQFP144 Package Pinout

|    |        |    |         |    |        |     |       |
|----|--------|----|---------|----|--------|-----|-------|
| 1  | PX00   | 37 | GND     | 73 | PA21   | 109 | GND   |
| 2  | PX01   | 38 | PX10    | 74 | PA22   | 110 | PX30  |
| 3  | PB20   | 39 | PA05    | 75 | PA23   | 111 | PB08  |
| 4  | PX02   | 40 | PX11    | 76 | PA24   | 112 | PX31  |
| 5  | PB21   | 41 | PA06    | 77 | PA25   | 113 | PB09  |
| 6  | PB22   | 42 | PX12    | 78 | PA26   | 114 | PX32  |
| 7  | VDDIO  | 43 | PA07    | 79 | PA27   | 115 | PB10  |
| 8  | GND    | 44 | PX13    | 80 | PA28   | 116 | VDDIO |
| 9  | PB23   | 45 | PA08    | 81 | VDDANA | 117 | GND   |
| 10 | PX03   | 46 | PX14    | 82 | ADVREF | 118 | PX33  |
| 11 | PB24   | 47 | PA09    | 83 | GNDANA | 119 | PB11  |
| 12 | PX04   | 48 | PA10    | 84 | VDDPLL | 120 | PX34  |
| 13 | PB25   | 49 | N/C     | 85 | PC00   | 121 | PB12  |
| 14 | PB26   | 50 | PA11    | 86 | PC01   | 122 | PA29  |
| 15 | PB27   | 51 | VDDCORE | 87 | PX20   | 123 | PA30  |
| 16 | VDDOUT | 52 | GND     | 88 | PB00   | 124 | PC02  |
| 17 | VDDIN  | 53 | PA12    | 89 | PX21   | 125 | PC03  |
| 18 | GND    | 54 | PA13    | 90 | PB01   | 126 | PB13  |
| 19 | PB28   | 55 | VDDCORE | 91 | PX22   | 127 | PB14  |
| 20 | PB29   | 56 | PA14    | 92 | VDDIO  | 128 | TMS   |
| 21 | PB30   | 57 | PA15    | 93 | VDDIO  | 129 | TCK   |

**Table 6-2.** VQFP144 Package Pinout

|    |         |    |       |     |       |     |         |
|----|---------|----|-------|-----|-------|-----|---------|
| 22 | PB31    | 58 | PA16  | 94  | GND   | 130 | TDO     |
| 23 | RESET_N | 59 | PX15  | 95  | PX23  | 131 | TDI     |
| 24 | PX05    | 60 | PA17  | 96  | PB02  | 132 | PC04    |
| 25 | PA00    | 61 | PX16  | 97  | PX24  | 133 | PC05    |
| 26 | PX06    | 62 | PA18  | 98  | PB03  | 134 | PB15    |
| 27 | PA01    | 63 | PX17  | 99  | PX25  | 135 | PX35    |
| 28 | GND     | 64 | PA19  | 100 | PB04  | 136 | PB16    |
| 29 | VDDCORE | 65 | PX18  | 101 | PX26  | 137 | PX36    |
| 30 | PA02    | 66 | PA20  | 102 | PB05  | 138 | VDDCORE |
| 31 | PX07    | 67 | PX19  | 103 | PX27  | 139 | PB17    |
| 32 | PA03    | 68 | VBUS  | 104 | PB06  | 140 | PX37    |
| 33 | PX08    | 69 | VDDIO | 105 | PX28  | 141 | PB18    |
| 34 | PA04    | 70 | DM    | 106 | PB07  | 142 | PX38    |
| 35 | PX09    | 71 | DP    | 107 | PX29  | 143 | PB19    |
| 36 | VDDIO   | 72 | GND   | 108 | VDDIO | 144 | PX39    |

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## 7. Power Considerations

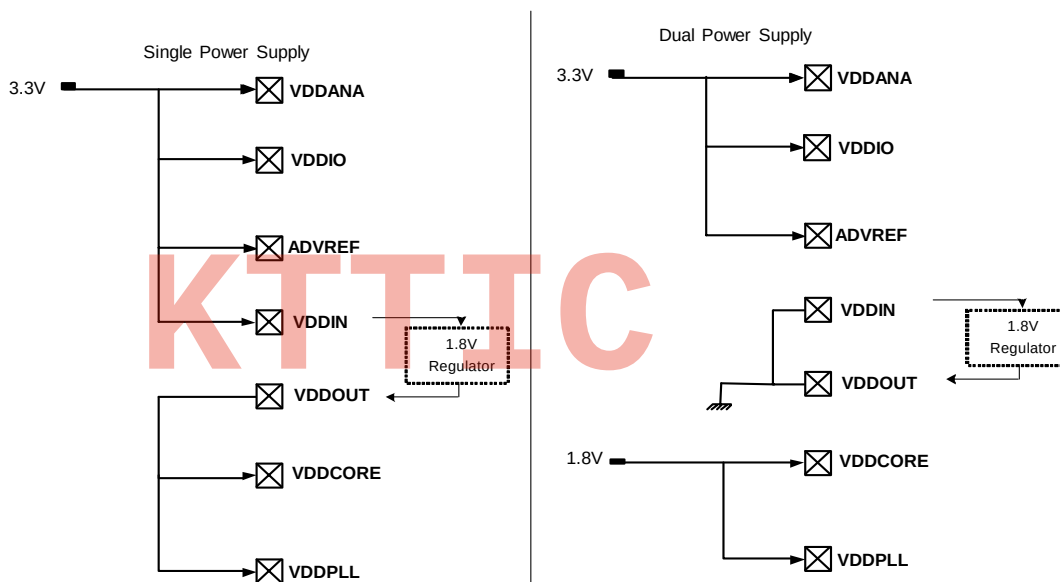
### 7.1 Power Supplies

The AT32UC3A has several types of power supply pins:

- **VDDIO:** Powers I/O lines. Voltage is 3.3V nominal.
- **VDDANA:** Powers the ADC. Voltage is 3.3V nominal.
- **VDDIN:** Input voltage for the voltage regulator. Voltage is 3.3V nominal.
- **VDDCORE:** Powers the core, memories, and peripherals. Voltage is 1.8V nominal.
- **VDDPLL:** Powers the PLL. Voltage is 1.8V nominal.

The ground pins GND are common to VDDCORE, VDDIO, VDDPLL. The ground pin for VDDANA is GNDANA.

Refer to "Power Consumption" on page 42 for power consumption on the various supply pins.





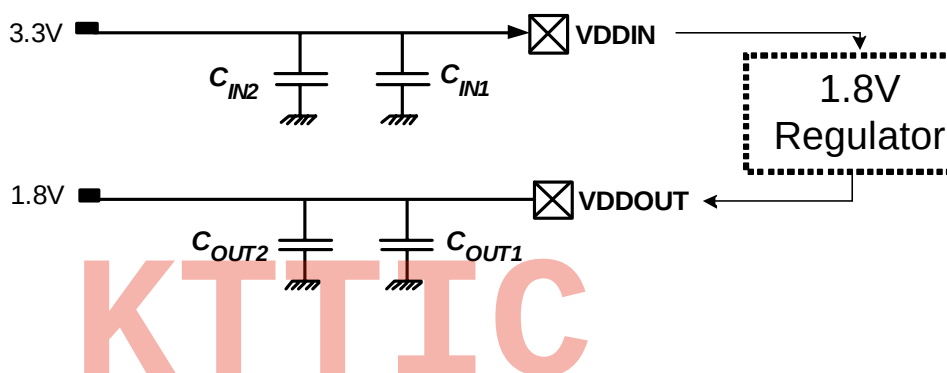
## 7.2 Voltage Regulator

### 7.2.1 Single Power Supply

The AT32UC3A embeds a voltage regulator that converts from 3.3V to 1.8V. The regulator takes its input voltage from VDDIN, and supplies the output voltage on VDDOUT. VDDOUT should be externally connected to the 1.8V domains.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. Two input decoupling capacitors must be placed close to the chip.

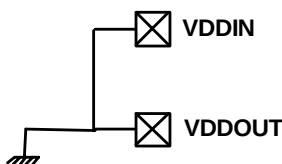
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel between VDDOUT and GND as close to the chip as possible



Refer to [Section 12.3 on page 41](#) for decoupling capacitors values and regulator characteristics

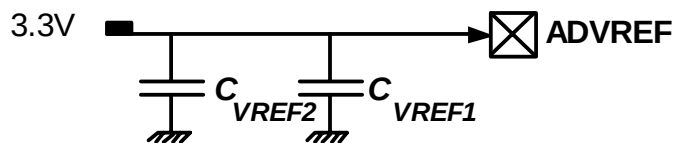
### 7.2.2 Dual Power Supply

In case of dual power supply, VDDIN and VDDOUT should be connected to ground to prevent from leakage current.



### 7.3 Analog-to-Digital Converter (A.D.C) reference.

The ADC reference (ADVREF) must be provided from an external source. Two decoupling capacitors must be used to insure proper decoupling.



Refer to [Section 12.4 on page 41](#) for decoupling capacitors values and electrical characteristics.

In case ADC is not used, the ADVREF pin should be connected to GND to avoid extra consumption.

# KTTIC

## 8. I/O Line Considerations

### 8.1 JTAG pins

TMS, TDI and TCK have pull-up resistors. TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

### 8.2 RESET\_N pin

The RESET\_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET\_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

### 8.3 TWI pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as PIO pins.

### 8.4 GPIO pins

All the I/O lines integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the GPIO Controllers. After reset, I/O lines default as inputs with pull-up resistors disabled, except when indicated otherwise in the column "Reset State" of the GPIO Controller multiplexing tables.

# KTTIC

## 9. Memories

### 9.1 Embedded Memories

- Internal High-Speed Flash
  - 512 KBytes (AT32UC3A0512, AT32UC3A1512)
  - 256 KBytes (AT32UC3A0256, AT32UC3A1256)
  - 128 KBytes (AT32UC3A1128, AT32UC3A2128)
    - 0 Wait State Access at up to 33 MHz in Worst Case Conditions
    - 1 Wait State Access at up to 66 MHz in Worst Case Conditions
    - Pipelined Flash Architecture, allowing burst reads from sequential Flash locations, hiding penalty of 1 wait state access
    - Pipelined Flash Architecture typically reduces the cycle penalty of 1 wait state operation to only 15% compared to 0 wait state operation
    - 100 000 Write Cycles, 15-year Data Retention Capability
    - 4 ms Page Programming Time, 8 ms Chip Erase Time
    - Sector Lock Capabilities, Bootloader Protection, Security Bit
    - 32 Fuses, Erased During Chip Erase
    - User Page For Data To Be Preserved During Chip Erase
- Internal High-Speed SRAM, Single-cycle access at full speed
  - 64 KBytes (AT32UC3A0512, AT32UC3A0256, AT32UC3A1512, AT32UC3A1256)
  - 32KBytes (AT32UC3A1128)

### 9.2 Physical Memory Map

The system bus is implemented as a bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even in boot. Note that AVR32 UC CPU uses unsegmented translation, as described in the AVR32 Architecture Manual. The 32-bit physical address space is mapped as follows:

**Table 9-1.** AT32UC3A Physical Memory Map

| Device                  | Start Address | Size         |              |              |              |              |              |
|-------------------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|
|                         |               | AT32UC3A0512 | AT32UC3A1512 | AT32UC3A0256 | AT32UC3A1256 | AT32UC3A0128 | AT32UC3A1128 |
| Embedded SRAM           | 0x0000_0000   | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     | 32 Kbyte     | 32 Kbyte     |
| Embedded Flash          | 0x8000_0000   | 512 Kbyte    | 512 Kbyte    | 256 Kbyte    | 256 Kbyte    | 128 Kbyte    | 128 Kbyte    |
| EBI SRAM CS0            | 0xC000_0000   | 16 Mbyte     | -            | 16 Mbyte     | -            | 16 Mbyte     | -            |
| EBI SRAM CS2            | 0xC800_0000   | 16 Mbyte     | -            | 16 Mbyte     | -            | 16 Mbyte     | -            |
| EBI SRAM CS3            | 0xCC00_0000   | 16 Mbyte     | -            | 16 Mbyte     | -            | 16 Mbyte     | -            |
| EBI SRAM CS1 /SDRAM CS0 | 0xD000_0000   | 128 Mbyte    | -            | 128 Mbyte    | -            | 128 Mbyte    | -            |
| USB Configuration       | 0xE000_0000   | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     |
| HSB-PB Bridge A         | 0xFFFFE_0000  | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     | 64 Kbyte     |
| HSB-PB Bridge B         | 0xFFFFF_0000  | 64 Kbyte     | 64 Kbyte     | 64 kByte     | 64 kByte     | 64 Kbyte     | 64 Kbyte     |

**Table 9-2.** Flash Memory Parameters

| Part Number  | Flash Size<br>(FLASH_PW) | Number of pages<br>(FLASH_P) | Page size<br>(FLASH_W) | General Purpose<br>Fuse bits<br>(FLASH_F) |
|--------------|--------------------------|------------------------------|------------------------|-------------------------------------------|
| AT32UC3A0512 | 512 Kbytes               | 1024                         | 128 words              | 32 fuses                                  |
| AT32UC3A1512 | 512 Kbytes               | 1024                         | 128 words              | 32 fuses                                  |
| AT32UC3A0256 | 256 Kbytes               | 512                          | 128 words              | 32 fuses                                  |
| AT32UC3A1256 | 256 Kbytes               | 512                          | 128 words              | 32 fuses                                  |
| AT32UC3A1128 | 128 Kbytes               | 64                           | 128 words              | 32 fuses                                  |
| AT32UC3A0128 | 128 Kbytes               | 64                           | 128 words              | 32 fuses                                  |

### 9.3 Bus Matrix Connections

Accesses to unused areas returns an error result to the master requesting such an access.

The bus matrix has the several masters and slaves. Each master has its own bus and its own decoder, thus allowing a different memory mapping per master. The master number in the table below can be used to index the HMATRIX control registers. For example, MCFG0 is associated with the CPU Data master interface.

**Table 9-3.** High Speed Bus masters

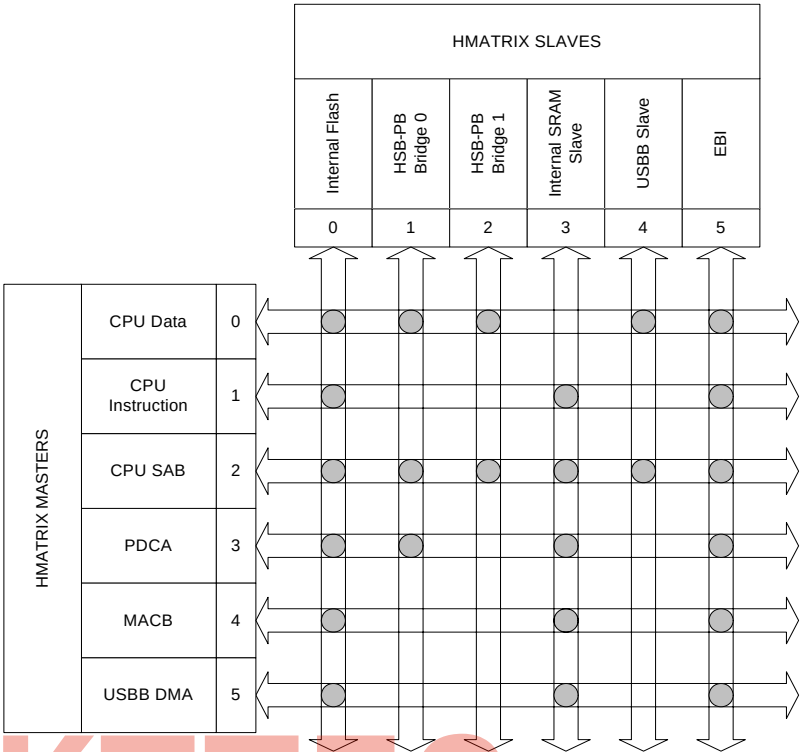
|          |                 |
|----------|-----------------|
| Master 0 | CPU Data        |
| Master 1 | CPU Instruction |
| Master 2 | CPU SAB         |
| Master 3 | PDCA            |
| Master 4 | MACB DMA        |
| Master 5 | USBB DMA        |

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with the Internal SRAM Slave Interface.

**Table 9-4.** High Speed Bus slaves

|         |                 |
|---------|-----------------|
| Slave 0 | Internal Flash  |
| Slave 1 | HSB-PB Bridge 0 |
| Slave 2 | HSB-PB Bridge 1 |
| Slave 3 | Internal SRAM   |
| Slave 4 | USBB DPRAM      |
| Slave 5 | EBI             |

Figure 9-1. HMatrix Master / Slave Connections



## 10. Peripherals

### 10.1 Peripheral address map

Table 10-1. Peripheral Address Mapping

| Address    |         | Peripheral Name                                                  | Bus |
|------------|---------|------------------------------------------------------------------|-----|
| 0xE0000000 | USBB    | USBB Slave Interface - USBB                                      | HSB |
| 0xFFFE0000 | USBB    | USBB Configuration Interface - USBB                              | PBB |
| 0xFFFE1000 | HMATRIX | HMATRIX Configuration Interface - HMATRIX                        | PBB |
| 0xFFFE1400 | FLASHC  | Flash Controller - FLASHC                                        | PBB |
| 0xFFFE1800 | MACB    | MACB Configuration Interface - MACB                              | PBB |
| 0xFFFE1C00 | SMC     | Static Memory Controller Configuration Interface - SMC           | PBB |
| 0xFFFE2000 | SDRAMC  | SDRAM Controller Configuration Interface - SDRAMC                | PBB |
| 0xFFFF0000 | PDCA    | Peripheral DMA Interface - PDCA                                  | PBA |
| 0xFFFF0800 | INTC    | Interrupt Controller Interface - INTC                            | PBA |
| 0xFFFF0C00 | PM      | Power Manager - PM                                               | PBA |
| 0xFFFF0D00 | RTC     | Real Time Clock - RTC                                            | PBA |
| 0xFFFF0D30 | WDT     | WatchDog Timer - WDT                                             | PBA |
| 0xFFFF0D80 | EIC     | External Interrupt Controller - EIC                              | PBA |
| 0xFFFF1000 | GPIO    | General Purpose IO Controller - GPIO                             | PBA |
| 0xFFFF1400 | USART0  | Universal Synchronous Asynchronous Receiver Transmitter - USART0 | PBA |
| 0xFFFF1800 | USART1  | Universal Synchronous Asynchronous Receiver Transmitter - USART1 | PBA |

Table 10-1. Peripheral Address Mapping (Continued)

| Address    | Peripheral Name |                                                                  | Bus |
|------------|-----------------|------------------------------------------------------------------|-----|
| 0xFFFF1C00 | USART2          | Universal Synchronous Asynchronous Receiver Transmitter - USART2 | PBA |
| 0xFFFF2000 | USART3          | Universal Synchronous Asynchronous Receiver Transmitter - USART3 | PBA |
| 0xFFFF2400 | SPI0            | Serial Peripheral Interface - SPI0                               | PBA |
| 0xFFFF2800 | SPI1            | Serial Peripheral Interface - SPI1                               | PBA |
| 0xFFFF2C00 | TWI             | Two Wire Interface - TWI                                         | PBA |
| 0xFFFF3000 | PWM             | Pulse Width Modulation Controller - PWM                          | PBA |
| 0xFFFF3400 | SSC             | Synchronous Serial Controller - SSC                              | PBA |
| 0xFFFF3800 | TC              | Timer/Counter - TC                                               | PBA |
| 0xFFFF3C00 | ADC             | Analog To Digital Converter - ADC                                | PBA |

10.2 CPU Local Bus Mapping

Some of the registers in the GPIO module are mapped onto the CPU local bus, in addition to being mapped on the Peripheral Bus. These registers can therefore be reached both by accesses on the Peripheral Bus, and by accesses on the local bus.

Mapping these registers on the local bus allows cycle-deterministic toggling of GPIO pins since the CPU and GPIO are the only modules connected to this bus. Also, since the local bus runs at CPU speed, one write or read operation can be performed per clock cycle to the local bus-mapped GPIO registers.



The following GPIO registers are mapped on the local bus:

**Table 10-2.** Local bus mapped GPIO registers

| Port | Register                             | Mode   | Local Bus Address | Access     |
|------|--------------------------------------|--------|-------------------|------------|
| 0    | Output Driver Enable Register (ODER) | WRITE  | 0x4000_0040       | Write-only |
|      |                                      | SET    | 0x4000_0044       | Write-only |
|      |                                      | CLEAR  | 0x4000_0048       | Write-only |
|      |                                      | TOGGLE | 0x4000_004C       | Write-only |
|      | Output Value Register (OVR)          | WRITE  | 0x4000_0050       | Write-only |
|      |                                      | SET    | 0x4000_0054       | Write-only |
|      |                                      | CLEAR  | 0x4000_0058       | Write-only |
|      |                                      | TOGGLE | 0x4000_005C       | Write-only |
|      | Pin Value Register (PVR)             | -      | 0x4000_0060       | Read-only  |
| 1    | Output Driver Enable Register (ODER) | WRITE  | 0x4000_0140       | Write-only |
|      |                                      | SET    | 0x4000_0144       | Write-only |
|      |                                      | CLEAR  | 0x4000_0148       | Write-only |
|      |                                      | TOGGLE | 0x4000_014C       | Write-only |
|      | Output Value Register (OVR)          | WRITE  | 0x4000_0150       | Write-only |
|      |                                      | SET    | 0x4000_0154       | Write-only |
|      |                                      | CLEAR  | 0x4000_0158       | Write-only |
|      |                                      | TOGGLE | 0x4000_015C       | Write-only |
|      | Pin Value Register (PVR)             | -      | 0x4000_0160       | Read-only  |
| 2    | Output Driver Enable Register (ODER) | WRITE  | 0x4000_0240       | Write-only |
|      |                                      | SET    | 0x4000_0244       | Write-only |
|      |                                      | CLEAR  | 0x4000_0248       | Write-only |
|      |                                      | TOGGLE | 0x4000_024C       | Write-only |
|      | Output Value Register (OVR)          | WRITE  | 0x4000_0250       | Write-only |
|      |                                      | SET    | 0x4000_0254       | Write-only |
|      |                                      | CLEAR  | 0x4000_0258       | Write-only |
|      |                                      | TOGGLE | 0x4000_025C       | Write-only |
|      | Pin Value Register (PVR)             | -      | 0x4000_0260       | Read-only  |

Table 10-2. Local bus mapped GPIO registers

| Port | Register                             | Mode   | Local Bus Address | Access     |
|------|--------------------------------------|--------|-------------------|------------|
| 3    | Output Driver Enable Register (ODER) | WRITE  | 0x4000_0340       | Write-only |
|      |                                      | SET    | 0x4000_0344       | Write-only |
|      |                                      | CLEAR  | 0x4000_0348       | Write-only |
|      |                                      | TOGGLE | 0x4000_034C       | Write-only |
|      | Output Value Register (OVR)          | WRITE  | 0x4000_0350       | Write-only |
|      |                                      | SET    | 0x4000_0354       | Write-only |
|      |                                      | CLEAR  | 0x4000_0358       | Write-only |
|      |                                      | TOGGLE | 0x4000_035C       | Write-only |
|      | Pin Value Register (PVR)             | -      | 0x4000_0360       | Read-only  |

10.3 Interrupt Request Signal Map

The various modules may output Interrupt request signals. These signals are routed to the Interrupt Controller (INTC), described in a later chapter. The Interrupt Controller supports up to 64 groups of interrupt requests. Each group can have up to 32 interrupt request signals. All interrupt signals in the same group share the same autovector address and priority level. Refer to the documentation for the individual submodules for a description of the semantics of the different interrupt requests.

The interrupt request signals are connected to the INTC as follows.

Table 10-3. Interrupt Request Signal Map

| Group | Line | Module                                          | Signal           |
|-------|------|-------------------------------------------------|------------------|
| 0     | 0    | AVR32 UC CPU with optional MPU and optional OCD | SYSBLOCK COMPARE |
| 1     | 0    | External Interrupt Controller                   | EIC 0            |
|       | 1    | External Interrupt Controller                   | EIC 1            |
|       | 2    | External Interrupt Controller                   | EIC 2            |
|       | 3    | External Interrupt Controller                   | EIC 3            |
|       | 4    | External Interrupt Controller                   | EIC 4            |
|       | 5    | External Interrupt Controller                   | EIC 5            |
|       | 6    | External Interrupt Controller                   | EIC 6            |
|       | 7    | External Interrupt Controller                   | EIC 7            |
|       | 8    | Real Time Counter                               | RTC              |
|       | 9    | Power Manager                                   | PM               |
|       | 10   | Frequency Meter                                 | FREQM            |

**Table 10-3.** Interrupt Request Signal Map

|   |    |                                                         |         |
|---|----|---------------------------------------------------------|---------|
| 2 | 0  | General Purpose Input/Output                            | GPIO 0  |
|   | 1  | General Purpose Input/Output                            | GPIO 1  |
|   | 2  | General Purpose Input/Output                            | GPIO 2  |
|   | 3  | General Purpose Input/Output                            | GPIO 3  |
|   | 4  | General Purpose Input/Output                            | GPIO 4  |
|   | 5  | General Purpose Input/Output                            | GPIO 5  |
|   | 6  | General Purpose Input/Output                            | GPIO 6  |
|   | 7  | General Purpose Input/Output                            | GPIO 7  |
|   | 8  | General Purpose Input/Output                            | GPIO 8  |
|   | 9  | General Purpose Input/Output                            | GPIO 9  |
|   | 10 | General Purpose Input/Output                            | GPIO 10 |
|   | 11 | General Purpose Input/Output                            | GPIO 11 |
|   | 12 | General Purpose Input/Output                            | GPIO 12 |
|   | 13 | General Purpose Input/Output                            | GPIO 13 |
| 3 | 0  | Peripheral DMA Controller                               | PDCA 0  |
|   | 1  | Peripheral DMA Controller                               | PDCA 1  |
|   | 2  | Peripheral DMA Controller                               | PDCA 2  |
|   | 3  | Peripheral DMA Controller                               | PDCA 3  |
|   | 4  | Peripheral DMA Controller                               | PDCA 4  |
|   | 5  | Peripheral DMA Controller                               | PDCA 5  |
|   | 6  | Peripheral DMA Controller                               | PDCA 6  |
|   | 7  | Peripheral DMA Controller                               | PDCA 7  |
|   | 8  | Peripheral DMA Controller                               | PDCA 8  |
|   | 9  | Peripheral DMA Controller                               | PDCA 9  |
|   | 10 | Peripheral DMA Controller                               | PDCA 10 |
|   | 11 | Peripheral DMA Controller                               | PDCA 11 |
|   | 12 | Peripheral DMA Controller                               | PDCA 12 |
|   | 13 | Peripheral DMA Controller                               | PDCA 13 |
|   | 14 | Peripheral DMA Controller                               | PDCA 14 |
| 4 | 0  | Flash Controller                                        | FLASHC  |
| 5 | 0  | Universal Synchronous/Asynchronous Receiver/Transmitter | USART0  |
| 6 | 0  | Universal Synchronous/Asynchronous Receiver/Transmitter | USART1  |
| 7 | 0  | Universal Synchronous/Asynchronous Receiver/Transmitter | USART2  |
| 8 | 0  | Universal Synchronous/Asynchronous Receiver/Transmitter | USART3  |

Table 10-3. Interrupt Request Signal Map

|    |   |                                   |        |
|----|---|-----------------------------------|--------|
| 9  | 0 | Serial Peripheral Interface       | SPI0   |
| 10 | 0 | Serial Peripheral Interface       | SPI1   |
| 11 | 0 | Two-wire Interface                | TWI    |
| 12 | 0 | Pulse Width Modulation Controller | PWM    |
| 13 | 0 | Synchronous Serial Controller     | SSC    |
| 14 | 0 | Timer/Counter                     | TC0    |
|    | 1 | Timer/Counter                     | TC1    |
|    | 2 | Timer/Counter                     | TC2    |
| 15 | 0 | Analog to Digital Converter       | ADC    |
| 16 | 0 | Ethernet MAC                      | MACB   |
| 17 | 0 | USB 2.0 OTG Interface             | USBB   |
| 18 | 0 | SDRAM Controller                  | SDRAMC |
| 19 | 0 | Audio Bitstream DAC               | DAC    |

10.4 Clock Connections

10.4.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 10-4. Timer/Counter clock connections

| Source   | Name         | Connection                       |
|----------|--------------|----------------------------------|
| Internal | TIMER_CLOCK1 | 32 KHz Oscillator                |
|          | TIMER_CLOCK2 | PBA clock / 2                    |
|          | TIMER_CLOCK3 | PBA clock / 8                    |
|          | TIMER_CLOCK4 | PBA clock / 32                   |
|          | TIMER_CLOCK5 | PBA clock / 128                  |
| External | XC0          | See <a href="#">Section 10.7</a> |
|          | XC1          |                                  |
|          | XC2          |                                  |

10.4.2 USARTs

Each USART can be connected to an internally divided clock:

Table 10-5. USART clock connections

| USART | Source   | Name    | Connection    |
|-------|----------|---------|---------------|
| 0     | Internal | CLK_DIV | PBA clock / 8 |
| 1     |          |         |               |
| 2     |          |         |               |
| 3     |          |         |               |

10.4.3 SPIs

Each SPI can be connected to an internally divided clock:

Table 10-6. SPI clock connections

| SPI | Source   | Name    | Connection                     |
|-----|----------|---------|--------------------------------|
| 0   | Internal | CLK_DIV | PBA clock or<br>PBA clock / 32 |
| 1   |          |         |                                |

10.5 Nexus OCD AUX port connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespectively of the PIO configuration. Two different OCD trace pin mappings are possible, depending on the configuration of the OCD AXS register. For details, see the AVR32 UC Technical Reference Manual.

Table 10-7. Nexus OCD AUX port connections

| Pin     | AXS=0 | AXS=1 |
|---------|-------|-------|
| EVTI_N  | PB19  | PA08  |
| MDO[5]  | PB16  | PA27  |
| MDO[4]  | PB14  | PA26  |
| MDO[3]  | PB13  | PA25  |
| MDO[2]  | PB12  | PA24  |
| MDO[1]  | PB11  | PA23  |
| MDO[0]  | PB10  | PA22  |
| EVTO_N  | PB20  | PB20  |
| MCKO    | PB21  | PA21  |
| MSEO[1] | PB04  | PA07  |
| MSEO[0] | PB17  | PA28  |

10.6 PDC handshake signals

The PDC and the peripheral modules communicate through a set of handshake signals. The following table defines the valid settings for the Peripheral Identifier (PID) in the PDC Peripheral Select Register (PSR).

Table 10-8. PDC Handshake Signals

| PID Value | Peripheral module & direction |
|-----------|-------------------------------|
| 0         | ADC                           |
| 1         | SSC - RX                      |
| 2         | USART0 - RX                   |
| 3         | USART1 - RX                   |

**Table 10-8.** PDC Handshake Signals

| PID Value | Peripheral module & direction |
|-----------|-------------------------------|
| 4         | USART2 - RX                   |
| 5         | USART3 - RX                   |
| 6         | TWI - RX                      |
| 7         | SPI0 - RX                     |
| 8         | SPI1 - RX                     |
| 9         | SSC - TX                      |
| 10        | USART0 - TX                   |
| 11        | USART1 - TX                   |
| 12        | USART2 - TX                   |
| 13        | USART3 - TX                   |
| 14        | TWI - TX                      |
| 15        | SPI0 - TX                     |
| 16        | SPI1 - TX                     |
| 17        | ABDAC                         |

## 10.7 Peripheral Multiplexing on I/O lines

Each GPIO line can be assigned to one of 3 peripheral functions; A, B or C. The following table define how the I/O lines on the peripherals A, B and C are multiplexed by the GPIO.

**Table 10-9.** GPIO Controller Function Multiplexing

| TQFP100 | VQFP144 | PIN  | GPIO Pin | Function A          | Function B      | Function C      |
|---------|---------|------|----------|---------------------|-----------------|-----------------|
| 19      | 25      | PA00 | GPIO 0   | USART0 - RXD        | TC - CLK0       |                 |
| 20      | 27      | PA01 | GPIO 1   | USART0 - TXD        | TC - CLK1       |                 |
| 23      | 30      | PA02 | GPIO 2   | USART0 - CLK        | TC - CLK2       |                 |
| 24      | 32      | PA03 | GPIO 3   | USART0 - RTS        | EIM - EXTINT[4] | DAC - DATA[0]   |
| 25      | 34      | PA04 | GPIO 4   | USART0 - CTS        | EIM - EXTINT[5] | DAC - DATAN[0]  |
| 26      | 39      | PA05 | GPIO 5   | USART1 - RXD        | PWM - PWM[4]    |                 |
| 27      | 41      | PA06 | GPIO 6   | USART1 - TXD        | PWM - PWM[5]    |                 |
| 28      | 43      | PA07 | GPIO 7   | USART1 - CLK        | PM - GCLK[0]    | SPI0 - NPCS[3]  |
| 29      | 45      | PA08 | GPIO 8   | USART1 - RTS        | SPI0 - NPCS[1]  | EIM - EXTINT[7] |
| 30      | 47      | PA09 | GPIO 9   | USART1 - CTS        | SPI0 - NPCS[2]  | MACB - WOL      |
| 31      | 48      | PA10 | GPIO 10  | SPI0 - NPCS[0]      | EIM - EXTINT[6] |                 |
| 33      | 50      | PA11 | GPIO 11  | SPI0 - MISO         | USB - USB_ID    |                 |
| 36      | 53      | PA12 | GPIO 12  | SPI0 - MOSI         | USB - USB_VBOF  |                 |
| 37      | 54      | PA13 | GPIO 13  | SPI0 - SCK          |                 |                 |
| 39      | 56      | PA14 | GPIO 14  | SSC - TX_FRAME_SYNC | SPI1 - NPCS[0]  | EBI - NCS[0]    |
| 40      | 57      | PA15 | GPIO 15  | SSC - TX_CLOCK      | SPI1 - SCK      | EBI - ADDR[20]  |

**Table 10-9.** GPIO Controller Function Multiplexing

|     |     |      |         |                     |                 |                |
|-----|-----|------|---------|---------------------|-----------------|----------------|
| 41  | 58  | PA16 | GPIO 16 | SSC - TX_DATA       | SPI1 - MOSI     | EBI - ADDR[21] |
| 42  | 60  | PA17 | GPIO 17 | SSC - RX_DATA       | SPI1 - MISO     | EBI - ADDR[22] |
| 43  | 62  | PA18 | GPIO 18 | SSC - RX_CLOCK      | SPI1 - NPCS[1]  | MACB - WOL     |
| 44  | 64  | PA19 | GPIO 19 | SSC - RX_FRAME_SYNC | SPI1 - NPCS[2]  |                |
| 45  | 66  | PA20 | GPIO 20 | EIM - EXTINT[8]     | SPI1 - NPCS[3]  |                |
| 51  | 73  | PA21 | GPIO 21 | ADC - AD[0]         | EIM - EXTINT[0] | USB - USB_ID   |
| 52  | 74  | PA22 | GPIO 22 | ADC - AD[1]         | EIM - EXTINT[1] | USB - USB_VBOF |
| 53  | 75  | PA23 | GPIO 23 | ADC - AD[2]         | EIM - EXTINT[2] | DAC - DATA[1]  |
| 54  | 76  | PA24 | GPIO 24 | ADC - AD[3]         | EIM - EXTINT[3] | DAC - DATAN[1] |
| 55  | 77  | PA25 | GPIO 25 | ADC - AD[4]         | EIM - SCAN[0]   | EBI - NCS[0]   |
| 56  | 78  | PA26 | GPIO 26 | ADC - AD[5]         | EIM - SCAN[1]   | EBI - ADDR[20] |
| 57  | 79  | PA27 | GPIO 27 | ADC - AD[6]         | EIM - SCAN[2]   | EBI - ADDR[21] |
| 58  | 80  | PA28 | GPIO 28 | ADC - AD[7]         | EIM - SCAN[3]   | EBI - ADDR[22] |
| 83  | 122 | PA29 | GPIO 29 | TWI - SDA           | USART2 - RTS    |                |
| 84  | 123 | PA30 | GPIO 30 | TWI - SCL           | USART2 - CTS    |                |
| 65  | 88  | PB00 | GPIO 32 | MACB - TX_CLK       | USART2 - RTS    | USART3 - RTS   |
| 66  | 90  | PB01 | GPIO 33 | MACB - TX_EN        | USART2 - CTS    | USART3 - CTS   |
| 70  | 96  | PB02 | GPIO 34 | MACB - TXD[0]       | DAC - DATA[0]   |                |
| 71  | 98  | PB03 | GPIO 35 | MACB - TXD[1]       | DAC - DATAN[0]  |                |
| 72  | 100 | PB04 | GPIO 36 | MACB - CRS          | USART3 - CLK    | EBI - NCS[3]   |
| 73  | 102 | PB05 | GPIO 37 | MACB - RXD[0]       | DAC - DATA[1]   |                |
| 74  | 104 | PB06 | GPIO 38 | MACB - RXD[1]       | DAC - DATAN[1]  |                |
| 75  | 106 | PB07 | GPIO 39 | MACB - RX_ER        |                 |                |
| 76  | 111 | PB08 | GPIO 40 | MACB - MDC          |                 |                |
| 77  | 113 | PB09 | GPIO 41 | MACB - MDIO         |                 |                |
| 78  | 115 | PB10 | GPIO 42 | MACB - TXD[2]       | USART3 - RXD    | EBI - SDCK     |
| 81  | 119 | PB11 | GPIO 43 | MACB - TXD[3]       | USART3 - TXD    | EBI - SDCKE    |
| 82  | 121 | PB12 | GPIO 44 | MACB - TX_ER        | TC - CLK0       | EBI - RAS      |
| 87  | 126 | PB13 | GPIO 45 | MACB - RXD[2]       | TC - CLK1       | EBI - CAS      |
| 88  | 127 | PB14 | GPIO 46 | MACB - RXD[3]       | TC - CLK2       | EBI - SDWE     |
| 95  | 134 | PB15 | GPIO 47 | MACB - RX_DV        |                 |                |
| 96  | 136 | PB16 | GPIO 48 | MACB - COL          | USB - USB_ID    | EBI - SDA10    |
| 98  | 139 | PB17 | GPIO 49 | MACB - RX_CLK       | USB - USB_VBOF  | EBI - ADDR[23] |
| 99  | 141 | PB18 | GPIO 50 | MACB - SPEED        | ADC - TRIGGER   | PWM - PWM[6]   |
| 100 | 143 | PB19 | GPIO 51 | PWM - PWM[0]        | PM - GCLK[0]    | EIM - SCAN[4]  |
| 1   | 3   | PB20 | GPIO 52 | PWM - PWM[1]        | PM - GCLK[1]    | EIM - SCAN[5]  |
| 2   | 5   | PB21 | GPIO 53 | PWM - PWM[2]        | PM - GCLK[2]    | EIM - SCAN[6]  |
| 3   | 6   | PB22 | GPIO 54 | PWM - PWM[3]        | PM - GCLK[3]    | EIM - SCAN[7]  |
| 6   | 9   | PB23 | GPIO 55 | TC - A0             | USART1 - DCD    |                |

**Table 10-9.** GPIO Controller Function Multiplexing

|    |     |      |          |                |               |              |
|----|-----|------|----------|----------------|---------------|--------------|
| 7  | 11  | PB24 | GPIO 56  | TC - B0        | USART1 - DSR  |              |
| 8  | 13  | PB25 | GPIO 57  | TC - A1        | USART1 - DTR  |              |
| 9  | 14  | PB26 | GPIO 58  | TC - B1        | USART1 - RI   |              |
| 10 | 15  | PB27 | GPIO 59  | TC - A2        | PWM - PWM[4]  |              |
| 14 | 19  | PB28 | GPIO 60  | TC - B2        | PWM - PWM[5]  |              |
| 15 | 20  | PB29 | GPIO 61  | USART2 - RXD   | PM - GCLK[1]  | EBI - NCS[2] |
| 16 | 21  | PB30 | GPIO 62  | USART2 - TXD   | PM - GCLK[2]  | EBI - SDCS   |
| 17 | 22  | PB31 | GPIO 63  | USART2 - CLK   | PM - GCLK[3]  | EBI - NWAIT  |
| 63 | 85  | PC00 | GPIO 64  |                |               |              |
| 64 | 86  | PC01 | GPIO 65  |                |               |              |
| 85 | 124 | PC02 | GPIO 66  |                |               |              |
| 86 | 125 | PC03 | GPIO 67  |                |               |              |
| 93 | 132 | PC04 | GPIO 68  |                |               |              |
| 94 | 133 | PC05 | GPIO 69  |                |               |              |
|    | 1   | PX00 | GPIO 100 | EBI - DATA[10] | USART0 - RXD  |              |
|    | 2   | PX01 | GPIO 99  | EBI - DATA[9]  | USART0 - TXD  |              |
|    | 4   | PX02 | GPIO 98  | EBI - DATA[8]  | USART0 - CTS  |              |
|    | 10  | PX03 | GPIO 97  | EBI - DATA[7]  | USART0 - RTS  |              |
|    | 12  | PX04 | GPIO 96  | EBI - DATA[6]  | USART1 - RXD  |              |
|    | 24  | PX05 | GPIO 95  | EBI - DATA[5]  | USART1 - TXD  |              |
|    | 26  | PX06 | GPIO 94  | EBI - DATA[4]  | USART1 - CTS  |              |
|    | 31  | PX07 | GPIO 93  | EBI - DATA[3]  | USART1 - RTS  |              |
|    | 33  | PX08 | GPIO 92  | EBI - DATA[2]  | USART3 - RXD  |              |
|    | 35  | PX09 | GPIO 91  | EBI - DATA[1]  | USART3 - TXD  |              |
|    | 38  | PX10 | GPIO 90  | EBI - DATA[0]  | USART2 - RXD  |              |
|    | 40  | PX11 | GPIO 109 | EBI - NWE1     | USART2 - TXD  |              |
|    | 42  | PX12 | GPIO 108 | EBI - NWE0     | USART2 - CTS  |              |
|    | 44  | PX13 | GPIO 107 | EBI - NRD      | USART2 - RTS  |              |
|    | 46  | PX14 | GPIO 106 | EBI - NCS[1]   |               | TC - A0      |
|    | 59  | PX15 | GPIO 89  | EBI - ADDR[19] | USART3 - RTS  | TC - B0      |
|    | 61  | PX16 | GPIO 88  | EBI - ADDR[18] | USART3 - CTS  | TC - A1      |
|    | 63  | PX17 | GPIO 87  | EBI - ADDR[17] |               | TC - B1      |
|    | 65  | PX18 | GPIO 86  | EBI - ADDR[16] |               | TC - A2      |
|    | 67  | PX19 | GPIO 85  | EBI - ADDR[15] | EIM - SCAN[0] | TC - B2      |
|    | 87  | PX20 | GPIO 84  | EBI - ADDR[14] | EIM - SCAN[1] | TC - CLK0    |
|    | 89  | PX21 | GPIO 83  | EBI - ADDR[13] | EIM - SCAN[2] | TC - CLK1    |
|    | 91  | PX22 | GPIO 82  | EBI - ADDR[12] | EIM - SCAN[3] | TC - CLK2    |
|    | 95  | PX23 | GPIO 81  | EBI - ADDR[11] | EIM - SCAN[4] |              |
|    | 97  | PX24 | GPIO 80  | EBI - ADDR[10] | EIM - SCAN[5] |              |



**Table 10-9.** GPIO Controller Function Multiplexing

|  |     |      |          |                |                |  |
|--|-----|------|----------|----------------|----------------|--|
|  | 99  | PX25 | GPIO 79  | EBI - ADDR[9]  | EIM - SCAN[6]  |  |
|  | 101 | PX26 | GPIO 78  | EBI - ADDR[8]  | EIM - SCAN[7]  |  |
|  | 103 | PX27 | GPIO 77  | EBI - ADDR[7]  | SPI0 - MISO    |  |
|  | 105 | PX28 | GPIO 76  | EBI - ADDR[6]  | SPI0 - MOSI    |  |
|  | 107 | PX29 | GPIO 75  | EBI - ADDR[5]  | SPI0 - SCK     |  |
|  | 110 | PX30 | GPIO 74  | EBI - ADDR[4]  | SPI0 - NPCS[0] |  |
|  | 112 | PX31 | GPIO 73  | EBI - ADDR[3]  | SPI0 - NPCS[1] |  |
|  | 114 | PX32 | GPIO 72  | EBI - ADDR[2]  | SPI0 - NPCS[2] |  |
|  | 118 | PX33 | GPIO 71  | EBI - ADDR[1]  | SPI0 - NPCS[3] |  |
|  | 120 | PX34 | GPIO 70  | EBI - ADDR[0]  | SPI1 - MISO    |  |
|  | 135 | PX35 | GPIO 105 | EBI - DATA[15] | SPI1 - MOSI    |  |
|  | 137 | PX36 | GPIO 104 | EBI - DATA[14] | SPI1 - SCK     |  |
|  | 140 | PX37 | GPIO 103 | EBI - DATA[13] | SPI1 - NPCS[0] |  |
|  | 142 | PX38 | GPIO 102 | EBI - DATA[12] | SPI1 - NPCS[1] |  |
|  | 144 | PX39 | GPIO 101 | EBI - DATA[11] | SPI1 - NPCS[2] |  |

## 10.8 Oscillator Pinout

The oscillators are not mapped to the normal A,B or C functions and their muxings are controlled by registers in the Power Manager (PM). Please refer to the power manager chapter for more information about this.

**Table 10-10.** Oscillator pinout

| TQFP100 pin | VQFP144 pin | Pad  | Oscillator pin |
|-------------|-------------|------|----------------|
| 85          | 124         | PC02 | xin0           |
| 93          | 132         | PC04 | xin1           |
| 63          | 85          | PC00 | xin32          |
| 86          | 125         | PC03 | xout0          |
| 94          | 133         | PC05 | xout1          |
| 64          | 86          | PC01 | xout32         |

## 10.9 USART Configuration

**Table 10-11.** USART Supported Mode

|        | SPI | RS485 | ISO7816 | IrDA | Modem | Manchester Encoding |
|--------|-----|-------|---------|------|-------|---------------------|
| USART0 | Yes | No    | No      | No   | No    | No                  |
| USART1 | Yes | Yes   | Yes     | Yes  | Yes   | Yes                 |
| USART2 | Yes | No    | No      | No   | No    | No                  |
| USART3 | Yes | No    | No      | No   | No    | No                  |

## 10.10 GPIO

The GPIO open drain feature (GPIO ODMER register (Open Drain Mode Enable Register)) is not available for this device.

## 10.11 Peripheral overview

### 10.11.1 External Bus Interface

- Optimized for Application Memory Space support
- Integrates Two External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
- Optimized External Bus:
  - 16-bit Data Bus
  - 24-bit Address Bus, Up to 16-Mbytes Addressable
  - Optimized pin multiplexing to reduce latencies on External Memories
- 4 SRAM Chip Selects, 1SDRAM Chip Select:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3

### 10.11.2 Static Memory Controller

- 4 Chip Selects Available
- 64-Mbyte Address Space per Chip Select
- 8-, 16-bit Data Bus
- Word, Halfword, Byte Transfers
- Byte Write or Byte Select Lines
- Programmable Setup, Pulse And Hold Time for Read Signals per Chip Select
- Programmable Setup, Pulse And Hold Time for Write Signals per Chip Select
- Programmable Data Float Time per Chip Select
- Compliant with LCD Module
- External Wait Request
- Automatic Switch to Slow Clock Mode
- Asynchronous Read in Page Mode Supported: Page Size Ranges from 4 to 32 Bytes

### 10.11.3 SDRAM Controller

- Numerous Configurations Supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with Two or Four Internal Banks
  - SDRAM with 16-bit Data Path
- Programming Facilities
  - Word, Half-word, Byte Access
  - Automatic Page Break When Memory Boundary Has Been Reached
  - Multibank Ping-pong Access
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable
- Energy-saving Capabilities
  - Self-refresh, Power-down and Deep Power Modes Supported

- Supports Mobile SDRAM Devices
- Error Detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by Software
- CAS Latency of 1, 2, 3 Supported
- Auto Precharge Command Not Used

#### 10.11.4 USB Controller

- USB 2.0 Compliant, Full-/Low-Speed (FS/LS) and On-The-Go (OTG), 12 Mbit/s
- 7 Pipes/Endpoints
- 960 bytes of Embedded Dual-Port RAM (DPRAM) for Pipes/Endpoints
- Up to 2 Memory Banks per Pipe/Endpoint (Not for Control Pipe/Endpoint)
- Flexible Pipe/Endpoint Configuration and Management with Dedicated DMA Channels
- On-Chip Transceivers Including Pull-Ups

#### 10.11.5 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to Peripheral Bus A (PBA) max frequency
  - The chip select line may be left active to speed up transfers on the same device

#### 10.11.6 Two-wire Interface

- High speed up to 400kbit/s
- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations

#### 10.11.7 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection

- Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- SPI Mode
  - Master or Slave
  - Serial Clock Programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to Internal Clock Frequency PBA/4
- Supports Connection of Two Peripheral DMA Controller Channels (PDC)
  - Offers Buffer Transfer without Processor Intervention

#### 10.11.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

#### 10.11.9 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

#### 10.11.10 Pulse Width Modulation Controller

- 7 channels, one 20-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock
  - Independent Period and Duty Cycle, with Double Bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

#### 10.11.11 Ethernet 10/100 MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 Mb/s per second data throughput capability
- Full- and half-duplex operations
- MII or RMI interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data

#### 10.11.12 Audio Bitstream DAC

- Digital Stereo DAC
- Oversampled D/A conversion architecture
  - Oversampling ratio fixed 128x
  - FIR equalization filter
  - Digital interpolation filter: Comb4
  - 3rd Order Sigma-Delta D/A converters
- Digital bitstream outputs
- Parallel interface
- Connected to Peripheral DMA Controller for background transfer without CPU intervention

KTTIC

## 11. Boot Sequence

This chapter summarizes the boot sequence of the AT32UC3A. The behaviour after power-up is controlled by the Power Manager. For specific details, refer to [Section 13. "Power Manager \(PM\)" on page 55](#).

### 11.1 Starting of clocks

After power-up, the device will be held in a reset state by the Power-On Reset circuitry, until the power has stabilized throughout the device. Once the power has stabilized, the device will use the internal RC Oscillator as clock source.

On system start-up, the PLLs are disabled. All clocks to all modules are running. No clocks have a divided frequency, all parts of the system receives a clock with the same frequency as the internal RC Oscillator.

### 11.2 Fetching of initial instructions

After reset has been released, the AVR32 UC CPU starts fetching instructions from the reset address, which is 0x8000\_0000. This address points to the first address in the internal Flash.

The code read from the internal Flash is free to configure the system to use for example the PLLs, to divide the frequency of the clock routed to some of the peripherals, and to gate the clocks to unused peripherals.

# KTTIC

12. Electrical Characteristics

12.1 Absolute Maximum Ratings\*

|                                                             |                 |
|-------------------------------------------------------------|-----------------|
| Operating Temperature.....                                  | -40°C to +85°C  |
| Storage Temperature .....                                   | -60°C to +150°C |
| Voltage on Input Pin<br>with respect to Ground-O.3V to 5.5V |                 |
| Maximum Operating Voltage (VDDCORE, VDDPLL) .....           | 1.95V           |
| Maximum Operating Voltage (VDDIO).....                      | 3.6V            |
| Total DC Output Current on all I/O Pin                      |                 |
| for TQFP100 packag .....                                    | 370 mA          |
| for LQGP144 package .....                                   | 470 mA          |

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

KTTIC

## 12.2 DC Characteristics

The following characteristics are applicable to the operating temperature range:  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise specified and are certified for a junction temperature up to  $T_J = 100^{\circ}\text{C}$ .

| Symbol                        | Parameter                            | Condition                                                 | Min.                       | Typ. | Max  | Units         |
|-------------------------------|--------------------------------------|-----------------------------------------------------------|----------------------------|------|------|---------------|
| $V_{VDDCORE}$                 | DC Supply Core                       |                                                           | 1.65                       |      | 1.95 | V             |
| $V_{VDDPLL}$                  | DC Supply PLL                        |                                                           | 1.65                       |      | 1.95 | V             |
| $V_{VDDIO}$                   | DC Supply Peripheral I/Os            |                                                           | 3.0                        |      | 3.6  | V             |
| $V_{REF}$                     | Analog reference voltage             |                                                           | 2.6                        |      | 3.6  | V             |
| $V_{IL}$                      | Input Low-level Voltage              |                                                           | -0.3                       |      | +0.8 | V             |
| $V_{IH}$                      | Input High-level Voltage             | All GPIOs except for PC00, PC01, PC02, PC03, PC04, PC05.  | 2.0                        |      | 5.5V | V             |
|                               |                                      | PC00, PC01, PC02, PC03, PC04, PC05.                       | 2.0                        |      | 3.6V | V             |
| $V_{OL}$                      | Output Low-level Voltage             | $I_{OL} = -4\text{mA}$                                    |                            |      | 0.4  | V             |
| $V_{OH}$                      | Output High-level Voltage            | $I_{OL} = 4\text{mA}$                                     | $V_{VDDIO} - 0.4$          |      |      | V             |
| $I_{LEAK}$                    | Input Leakage Current                | Pullup resistors disabled                                 |                            |      | 1    | $\mu\text{A}$ |
| $C_{IN}$<br>Input Capacitance |                                      | TQFP100 Package                                           |                            | 7    |      | pF            |
|                               |                                      | LQFP144 Package                                           |                            | 7    |      | pF            |
| $R_{PULLUP}$                  | Pull-up Resistance                   |                                                           | 10K                        |      |      | Ohm           |
| $I_O$                         | Output Current                       |                                                           |                            | 4    |      | mA            |
| $I_{SC}$                      | Static Current                       | On $V_{VDDCORE} = 1.8\text{V}$ ,<br>CPU is in static mode | $T_A = 25^{\circ}\text{C}$ | TBD  |      | $\mu\text{A}$ |
|                               |                                      | All inputs driven;<br>RESET_N=1,                          | $T_A = 85^{\circ}\text{C}$ | TBD  | TBD  | $\mu\text{A}$ |
| $I_{SCR}$                     | Static Current of internal regulator | Low Power mode (stop, deep stop or static)                | $T_A = 25^{\circ}\text{C}$ | 10   |      | $\mu\text{A}$ |



## 12.3 Regulator characteristics

### 12.3.1 Electrical characteristics

| Symbol      | Parameter                                        | Condition | Min. | Typ. | Max. | Units |
|-------------|--------------------------------------------------|-----------|------|------|------|-------|
| $V_{DDIN}$  | Supply voltage (input)                           |           | 2.7  | 3.3  | 3.6  | V     |
| $V_{DDOUT}$ | Supply voltage (output)                          |           | 1.81 | 1.85 | 1.89 | V     |
| $I_{OUT}$   | Maximum DC output current with $V_{DDIN} = 3.3V$ |           |      |      | 100  | mA    |
|             | Maximum DC output current with $V_{DDIN} = 2.7V$ |           |      |      | 90   | mA    |

### 12.3.2 Decoupling requirements

| Symbol     | Parameter                    | Condition | Typ. | Techno. | Units |
|------------|------------------------------|-----------|------|---------|-------|
| $C_{IN1}$  | Input Regulator Capacitor 1  |           | 1    | NPO     | nF    |
| $C_{IN2}$  | Input Regulator Capacitor 2  |           | 4.7  | X7R     | uF    |
| $C_{OUT1}$ | Output Regulator Capacitor 1 |           | 470  | NPO     | pF    |
| $C_{OUT2}$ | Output Regulator Capacitor 2 |           | 2.2  | X7R     | uF    |

## 12.4 Analog characteristics

### 12.4.1 Electrical characteristics

| Symbol       | Parameter                        | Condition | Min. | Typ. | Max. | Units |
|--------------|----------------------------------|-----------|------|------|------|-------|
| $V_{ADVREF}$ | Analog voltage reference (input) |           | 2.6  |      | 3.6  | V     |

### 12.4.2 Decoupling requirements

| Symbol      | Parameter                     | Condition | Typ. | Techno. | Units |
|-------------|-------------------------------|-----------|------|---------|-------|
| $C_{VREF1}$ | Voltage reference Capacitor 1 |           | 10   | -       | nF    |
| $C_{VREF2}$ | Voltage reference Capacitor 2 |           | 1    | -       | uF    |

### 12.4.3 BOD

Table 12-1. BODLEVEL Values

| BODLEVEL Value | Typ. | Units. |
|----------------|------|--------|
| 000000b        | 1.58 | V      |
| 010111b        | 1.62 | V      |
| 011111b        | 1.67 | V      |
| 100111b        | 1.77 | V      |
| 111111b        | 1.92 | V      |

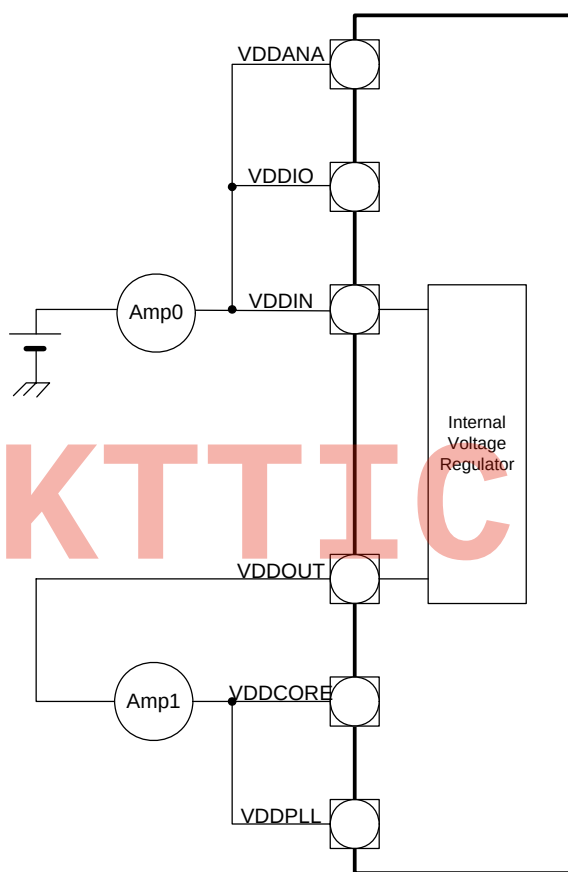
The values in Table 12-1 describes the values of the BODLEVEL in the flash FGPFRR register.

## 12.5 Power Consumption

The values in Table 12-2 and Table 12-3 on page 43 are measured values of power consumption with operating conditions as follows:

- $V_{DDIO} = 3.3V$
- $V_{DDCORE} = V_{DDPLL} = 1.8V$
- $T_A = 25^{\circ}C, T_A = 85^{\circ}C$
- I/Os are inactive

**Figure 12-1.** Measurement setup



These figures represent the power consumption measured on the power supplies.

**Table 12-2.** Power Consumption for Different Modes<sup>(1)</sup>

| Mode   | Conditions                                                                                                                                                                                                                                                                            |            | Consumption<br>Typ. | Unit |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---------------------|------|
| Active | CPU running from flash.<br>CPU clocked from PLL0 at f MHz<br>Voltage regulator is on.<br>XIN0 : external clock. <sup>(1)</sup><br>XIN1 stopped. XIN32 stopped<br>PLL0 running<br>All peripheral clocks activated.<br>GPIOs on internal pull-up.<br>JTAG unconnected with ext pull-up. | f = 12 MHz | 9                   | mA   |
|        |                                                                                                                                                                                                                                                                                       | f = 24 MHz | 16                  | mA   |
|        |                                                                                                                                                                                                                                                                                       | f = 36MHz  | 23                  | mA   |
|        |                                                                                                                                                                                                                                                                                       | f = 50 MHz | 31.5                | mA   |
|        |                                                                                                                                                                                                                                                                                       | f = 60 MHz | 37                  | mA   |
| Static | Typ : Ta = 25 °C<br>CPU is in static mode<br>GPIOs on internal pull-up.<br>All peripheral clocks de-activated.<br>DM and DP pins connected to ground.<br>XIN0,Xin1 and XIN2 are stopped                                                                                               | on Amp0    | 25                  | uA   |
|        |                                                                                                                                                                                                                                                                                       | on Amp1    | 14                  | uA   |

1. Core frequency is generated from XIN0 using the PLL so that 140 MHz < fpll0 < 160 MHz and 10 MHz < fxin0 < 12MHz

**Table 12-3.** Power Consumption by Peripheral in Active Mode

| Peripheral | Consumption | Unit   |
|------------|-------------|--------|
| GPIO       | 37          | μA/MHz |
| SMC        | 10          |        |
| SDRAMC     | 4           |        |
| ADC        | 18          |        |
| EBI        | 31          |        |
| INTC       | 25          |        |
| TWI        | 14          |        |
| MACB       | 45          |        |
| PDCA       | 30          |        |
| PWM        | 36          |        |
| RTC        | 7           |        |
| SPI        | 13          |        |
| SSC        | 13          |        |
| TC         | 10          |        |
| USART      | 35          |        |
| USB        | 45          |        |

## 12.6 Clock Characteristics

These parameters are given in the following conditions:

- $V_{DDCORE} = 1.8V$
- Ambient Temperature = 25°C

### 12.6.1 CPU/HSB Clock Characteristics

**Table 12-4.** Core Clock Waveform Parameters

| Symbol          | Parameter           | Conditions | Min   | Max | Units |
|-----------------|---------------------|------------|-------|-----|-------|
| $1/(t_{CPCPU})$ | CPU Clock Frequency |            |       | 66  | MHz   |
| $t_{CPCPU}$     | CPU Clock Period    |            | 15,15 |     | ns    |

### 12.6.2 PBA Clock Characteristics

**Table 12-5.** PBA Clock Waveform Parameters

| Symbol          | Parameter           | Conditions | Min   | Max | Units |
|-----------------|---------------------|------------|-------|-----|-------|
| $1/(t_{CPPBA})$ | PBA Clock Frequency |            |       | 66  | MHz   |
| $t_{CPPBA}$     | PBA Clock Period    |            | 15,15 |     | ns    |

### 12.6.3 PBB Clock Characteristics

**Table 12-6.** PBB Clock Waveform Parameters

| Symbol          | Parameter           | Conditions | Min   | Max | Units |
|-----------------|---------------------|------------|-------|-----|-------|
| $1/(t_{CPPBB})$ | PBB Clock Frequency |            |       | 66  | MHz   |
| $t_{CPPBB}$     | PBB Clock Period    |            | 15,15 |     | ns    |

### 12.6.4 XIN Clock Characteristics

**Table 12-7.** XIN Clock Electrical Characteristics

| Symbol          | Parameter                  | Conditions     | Min                    | Max                    | Units |
|-----------------|----------------------------|----------------|------------------------|------------------------|-------|
| $1/(t_{CPXIN})$ | XIN Clock Frequency        | External clock |                        | 50                     | MHz   |
|                 |                            | Crystal        | 3                      | 20                     | MHz   |
| $t_{CHXIN}$     | XIN Clock High Half-period |                | $0.4 \times t_{CPXIN}$ | $0.6 \times t_{CPXIN}$ |       |
| $t_{CLXIN}$     | XIN Clock Low Half-period  |                | $0.4 \times t_{CPXIN}$ | $0.6 \times t_{CPXIN}$ |       |
| $C_{IN}$        | XIN Input Capacitance      |                |                        | TBD                    | pF    |

## 12.7 Crystal Oscillator Characteristics

The following characteristics are applicable to the operating temperature range:  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  and worst case of power supply, unless otherwise specified.

### 12.7.1 32 KHz Oscillator Characteristics

**Table 12-8.** 32 KHz Oscillator Characteristics

| Symbol            | Parameter                    | Conditions                                | Min | Typ | Max         | Unit    |
|-------------------|------------------------------|-------------------------------------------|-----|-----|-------------|---------|
| $1/(t_{CP32KHz})$ | Crystal Oscillator Frequency |                                           |     |     | 32 768      | Hz      |
|                   | Duty Cycle                   |                                           | 40  | 50  | 60          | %       |
| $C_L$             | Equivalent Load Capacitance  |                                           | 6   |     | 12.5        | pF      |
| $t_{ST}$          | Startup Time                 | $C_L = 6pF^{(1)}$<br>$C_L = 12.5pF^{(1)}$ |     |     | 600<br>1200 | ms      |
| $I_{OSC}$         | Current Consumption          | Active mode                               |     |     | 1.8         | $\mu A$ |
|                   |                              | Standby mode                              |     |     | 0.1         | $\mu A$ |

Note: 1.  $C_L$  is the equivalent load capacitance.

### 12.7.2 Main Oscillators Characteristics

**Table 12-9.** Main Oscillator Characteristics

| Symbol           | Parameter                                          | Conditions           | Min  | Typ | Max | Unit    |
|------------------|----------------------------------------------------|----------------------|------|-----|-----|---------|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency                       |                      | 0.45 |     | 16  | MHz     |
| $C_{L1}, C_{L2}$ | Internal Load Capacitance<br>( $C_{L1} = C_{L2}$ ) |                      |      | 12  |     | pF      |
| $C_L$            | Equivalent Load Capacitance                        |                      |      | TBD |     | pF      |
|                  | Duty Cycle                                         |                      | 40   | 50  | 60  | %       |
| $t_{ST}$         | Startup Time                                       |                      |      |     | TBD | ms      |
| $I_{OSC}$        | Current Consumption                                | Active mode @TBD MHz |      |     | TBD | $\mu A$ |
|                  |                                                    | Standby mode @TBD V  |      |     | TBD | $\mu A$ |

Notes: 1.  $C_S$  is the shunt capacitance

### 12.7.3 PLL Characteristics

**Table 12-10.** Phase Lock Loop Characteristics

| Symbol    | Parameter           | Conditions   | Min | Typ | Max | Unit    |
|-----------|---------------------|--------------|-----|-----|-----|---------|
| $F_{OUT}$ | Output Frequency    |              | 80  |     | 240 | MHz     |
| $F_{IN}$  | Input Frequency     |              | TBD |     | TBD | MHz     |
| $I_{PLL}$ | Current Consumption | active mode  |     |     | TBD | mA      |
|           |                     | standby mode |     |     | TBD | $\mu A$ |

## 12.8 ADC Characteristics

**Table 12-11.** Channel Conversion Time and ADC Clock

| Parameter                       | Conditions             | Min | Typ | Max                | Units |
|---------------------------------|------------------------|-----|-----|--------------------|-------|
| ADC Clock Frequency             | 10-bit resolution mode |     |     | 5                  | MHz   |
| ADC Clock Frequency             | 8-bit resolution mode  |     |     | 8                  | MHz   |
| Startup Time                    | Return from Idle Mode  |     |     | 20                 | μs    |
| Track and Hold Acquisition Time |                        | 600 |     |                    | ns    |
| Conversion Time                 | ADC Clock = 5 MHz      |     |     | 2                  | μs    |
| Conversion Time                 | ADC Clock = 8 MHz      |     |     | 1.25               | μs    |
| Throughput Rate                 | ADC Clock = 5 MHz      |     |     | 384 <sup>(1)</sup> | kSPS  |
| Throughput Rate                 | ADC Clock = 8 MHz      |     |     | 533 <sup>(2)</sup> | kSPS  |

Notes: 1. Corresponds to 13 clock cycles at 5 MHz: 3 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.  
 2. Corresponds to 15 clock cycles at 8 MHz: 5 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.

**Table 12-12.** External Voltage Reference Input

| Parameter                     | Conditions                           | Min | Typ | Max    | Units |
|-------------------------------|--------------------------------------|-----|-----|--------|-------|
| ADVREF Input Voltage Range    |                                      | 2.6 |     | VDDANA | V     |
| ADVREF Average Current        | On 13 samples with ADC Clock = 5 MHz |     | 200 | 250    | μA    |
| Current Consumption on VDDANA |                                      |     |     | TBD    | mA    |

**Table 12-13.** Analog Inputs

| Parameter             | Min | Typ | Max                 | Units |
|-----------------------|-----|-----|---------------------|-------|
| Input Voltage Range   | 0   |     | V <sub>ADVREF</sub> |       |
| Input Leakage Current |     | TBD |                     | μA    |
| Input Capacitance     |     |     | TBD                 | pF    |

**Table 12-14.** Transfer Characteristics

| Parameter                  | Conditions | Min  | Typ  | Max | Units |
|----------------------------|------------|------|------|-----|-------|
| Resolution                 |            |      | 10   |     | Bit   |
| Absolute Accuracy          | f=5MHz     |      |      | 0.8 | LSB   |
| Integral Non-linearity     | f=5MHz     |      | 0.35 | 0.5 | LSB   |
| Differential Non-linearity | f=5MHz     |      | 0.3  | 0.5 | LSB   |
| Offset Error               | f=5MHz     | -0.5 |      | 0.5 | LSB   |
| Gain Error                 | f=5MHz     | -0.5 |      | 0.5 | LSB   |

## 12.9 EBI Timings

These timings are given for worst case process, T = 85°C, VDDCORE = 1.65V, VDDIO = 3V and 40 pF load capacitance.

**Table 12-15.** SMC Clock Signal.

| Symbol                  | Parameter                      | Max <sup>(1)</sup>      | Units |
|-------------------------|--------------------------------|-------------------------|-------|
| 1/(t <sub>CPSMC</sub> ) | SMC Controller Clock Frequency | 1/(t <sub>CPCPU</sub> ) | MHz   |

Note: 1. The maximum frequency of the SMC interface is the same as the max frequency for the HSB.

**Table 12-16.** SMC Read Signals with Hold Settings

| Symbol                         | Parameter                                  | Min                                                               | Units |
|--------------------------------|--------------------------------------------|-------------------------------------------------------------------|-------|
| NRD Controlled (READ_MODE = 1) |                                            |                                                                   |       |
| SMC <sub>1</sub>               | Data Setup before NRD High                 | 12                                                                | ns    |
| SMC <sub>2</sub>               | Data Hold after NRD High                   | 0                                                                 |       |
| SMC <sub>3</sub>               | NRD High to NBS0/A0 Change <sup>(1)</sup>  | nrd hold length * t <sub>CPSMC</sub> - 1.3                        |       |
| SMC <sub>4</sub>               | NRD High to NBS1 Change <sup>(1)</sup>     | nrd hold length * t <sub>CPSMC</sub> - 1.3                        |       |
| SMC <sub>5</sub>               | NRD High to NBS2/A1 Change <sup>(1)</sup>  | nrd hold length * t <sub>CPSMC</sub> - 1.3                        |       |
| SMC <sub>6</sub>               | NRD High to NBS3 Change <sup>(1)</sup>     | nrd hold length * t <sub>CPSMC</sub> - 1.3                        |       |
| SMC <sub>7</sub>               | NRD High to A2 - A25 Change <sup>(1)</sup> | nrd hold length * t <sub>CPSMC</sub> - 1.3                        |       |
| SMC <sub>8</sub>               | NRD High to NCS Inactive <sup>(1)</sup>    | (nrd hold length - ncs rd hold length) * t <sub>CPSMC</sub> - 2.3 |       |
| SMC <sub>9</sub>               | NRD Pulse Width                            | nrd pulse length * t <sub>CPSMC</sub> - 1.4                       |       |
| NRD Controlled (READ_MODE = 0) |                                            |                                                                   |       |
| SMC <sub>10</sub>              | Data Setup before NCS High                 | 11.5                                                              | ns    |
| SMC <sub>11</sub>              | Data Hold after NCS High                   | 0                                                                 |       |
| SMC <sub>12</sub>              | NCS High to NBS0/A0 Change <sup>(1)</sup>  | ncs rd hold length * t <sub>CPSMC</sub> - 2.3                     |       |
| SMC <sub>13</sub>              | NCS High to NBS0/A0 Change <sup>(1)</sup>  | ncs rd hold length * t <sub>CPSMC</sub> - 2.3                     |       |
| SMC <sub>14</sub>              | NCS High to NBS2/A1 Change <sup>(1)</sup>  | ncs rd hold length * t <sub>CPSMC</sub> - 2.3                     |       |
| SMC <sub>15</sub>              | NCS High to NBS3 Change <sup>(1)</sup>     | ncs rd hold length * t <sub>CPSMC</sub> - 2.3                     |       |
| SMC <sub>16</sub>              | NCS High to A2 - A25 Change <sup>(1)</sup> | ncs rd hold length * t <sub>CPSMC</sub> - 4                       |       |
| SMC <sub>17</sub>              | NCS High to NRD Inactive <sup>(1)</sup>    | ncs rd hold length - nrd hold length)* t <sub>CPSMC</sub> - 1.3   |       |
| SMC <sub>18</sub>              | NCS Pulse Width                            | ncs rd pulse length * t <sub>CPSMC</sub> - 3.6                    |       |

Note: 1. hold length = total cycle duration - setup duration - pulse duration. "hold length" is for "ncs rd hold length" or "nrd hold length".

**Table 12-17.** SMC Read Signals with no Hold Settings

| Symbol                         | Parameter                  | Min  | Units |
|--------------------------------|----------------------------|------|-------|
| NRD Controlled (READ_MODE = 1) |                            |      |       |
| SMC <sub>19</sub>              | Data Setup before NRD High | 13.7 | ns    |
| SMC <sub>20</sub>              | Data Hold after NRD High   | 1    |       |
| NRD Controlled (READ_MODE = 0) |                            |      |       |
| SMC <sub>21</sub>              | Data Setup before NCS High | 13.3 | ns    |
| SMC <sub>22</sub>              | Data Hold after NCS High   | 0    |       |

**Table 12-18.** SMC Write Signals with Hold Settings

| Symbol                         | Parameter                                    | Min                                                                        | Units |
|--------------------------------|----------------------------------------------|----------------------------------------------------------------------------|-------|
| NRD Controlled (READ_MODE = 1) |                                              |                                                                            |       |
| SMC <sub>23</sub>              | Data Out Valid before NWE High               | $(nwe \text{ pulse length} - 1) * t_{CPSMC} - 0.9$                         | ns    |
| SMC <sub>24</sub>              | Data Out Valid after NWE High <sup>(1)</sup> | $nwe \text{ hold length} * t_{CPSMC} - 6$                                  |       |
| SMC <sub>25</sub>              | NWE High to NBS0/A0 Change <sup>(1)</sup>    | $nwe \text{ hold length} * t_{CPSMC} - 1.9$                                |       |
| SMC <sub>26</sub>              | NWE High to NBS1 Change <sup>(1)</sup>       | $nwe \text{ hold length} * t_{CPSMC} - 1.9$                                |       |
| SMC <sub>29</sub>              | NWE High to NBS2/A1 Change <sup>(1)</sup>    | $nwe \text{ hold length} * t_{CPSMC} - 1.9$                                |       |
| SMC <sub>30</sub>              | NWE High to NBS3 Change <sup>(1)</sup>       | $nwe \text{ hold length} * t_{CPSMC} - 1.9$                                |       |
| SMC <sub>31</sub>              | NWE High to A2 - A25 Change <sup>(1)</sup>   | $nwe \text{ hold length} * t_{CPSMC} - 1.7$                                |       |
| SMC <sub>32</sub>              | NWE High to NCS Inactive <sup>(1)</sup>      | $(nwe \text{ hold length} - ncs \text{ wr hold length}) * t_{CPSMC} - 2.9$ |       |
| SMC <sub>33</sub>              | NWE Pulse Width                              | $nwe \text{ pulse length} * t_{CPSMC} - 0.9$                               |       |
| NRD Controlled (READ_MODE = 0) |                                              |                                                                            |       |
| SMC <sub>34</sub>              | Data Out Valid before NCS High               | $(ncs \text{ wr pulse length} - 1) * t_{CPSMC} - 4.6$                      | ns    |
| SMC <sub>35</sub>              | Data Out Valid after NCS High <sup>(1)</sup> | $ncs \text{ wr hold length} * t_{CPSMC} - 5.8$                             |       |
| SMC <sub>36</sub>              | NCS High to NWE Inactive <sup>(1)</sup>      | $(ncs \text{ wr hold length} - nwe \text{ hold length}) * t_{CPSMC} - 0.6$ |       |

Note: 1. hold length = total cycle duration - setup duration - pulse duration. "hold length" is for "ncs wr hold length" or "nwe hold length"



Table 12-19. SMC Write Signals with No Hold Settings (NWE Controlled only).

| Symbol            | Parameter                        | Min                                               | Units |
|-------------------|----------------------------------|---------------------------------------------------|-------|
| SMC <sub>37</sub> | NWE Rising to A2-A25 Valid       | 5.4                                               | ns    |
| SMC <sub>38</sub> | NWE Rising to NBS0/A0 Valid      | 5                                                 |       |
| SMC <sub>39</sub> | NWE Rising to NBS1 Change        | 5                                                 |       |
| SMC <sub>40</sub> | NWE Rising to A1/NBS2 Change     | 5                                                 |       |
| SMC <sub>41</sub> | NWE Rising to NBS3 Change        | 5                                                 |       |
| SMC <sub>42</sub> | NWE Rising to NCS Rising         | 5.1                                               |       |
| SMC <sub>43</sub> | Data Out Valid before NWE Rising | (nwe pulse length - 1) * t <sub>CPSMC</sub> - 1.2 |       |
| SMC <sub>44</sub> | Data Out Valid after NWE Rising  | 5                                                 |       |
| SMC <sub>45</sub> | NWE Pulse Width                  | nwe pulse length * t <sub>CPSMC</sub> - 0.9       |       |

Figure 12-2. SMC Signals for NCS Controlled Accesses.

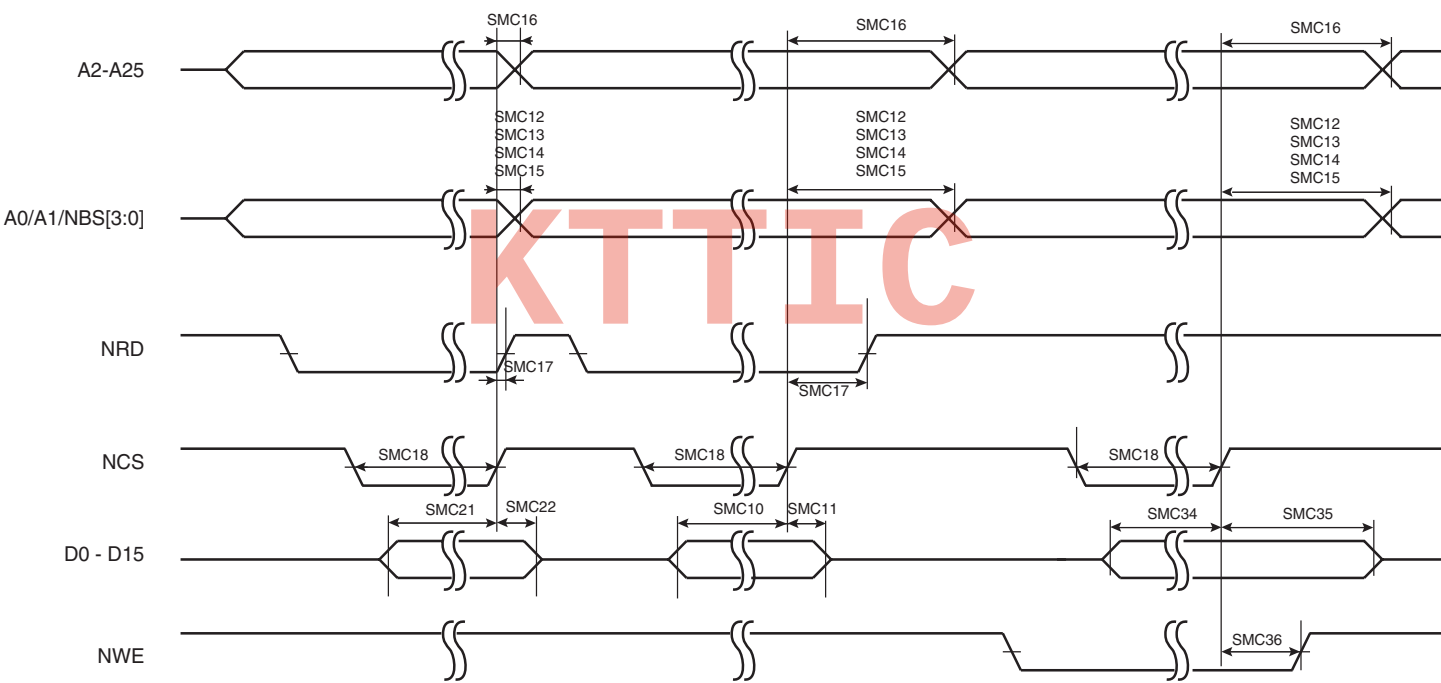
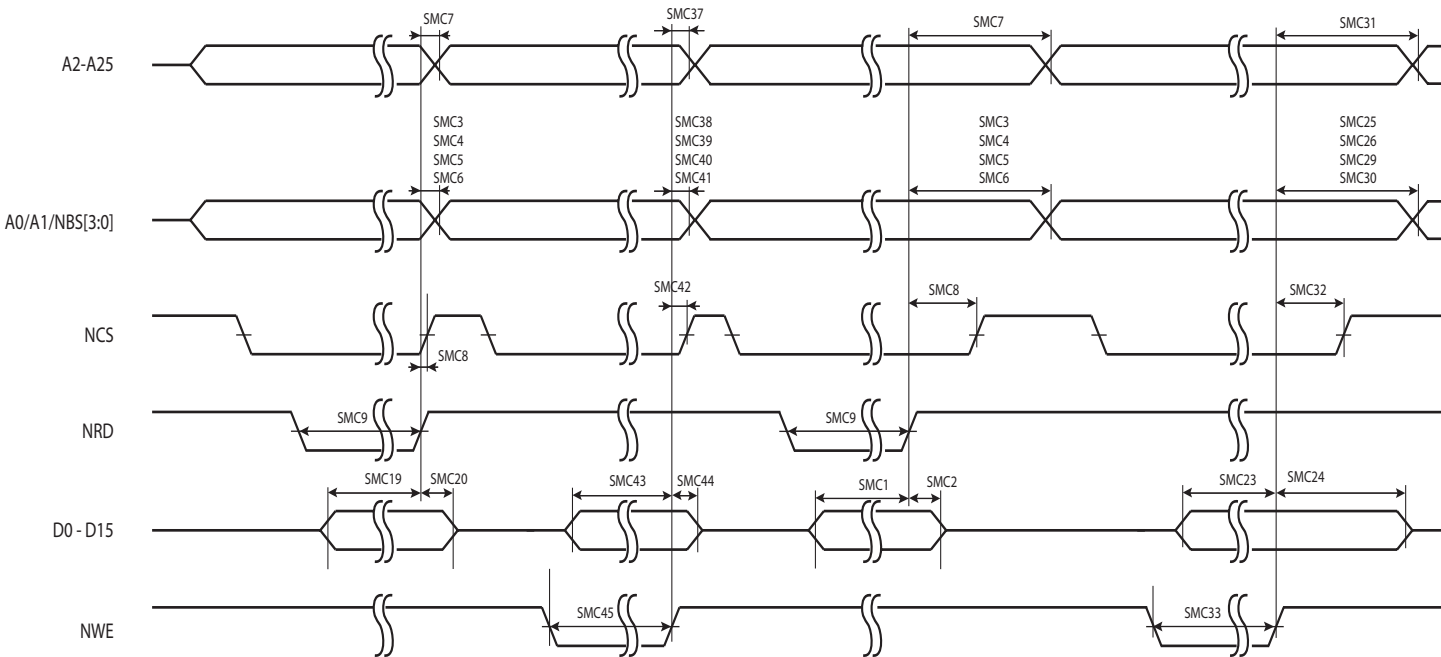


Figure 12-3. SMC Signals for NRD and NRW Controlled Accesses.



12.9.1 SDRAM Signals

These timings are given for 10 pF load on SDCK and 40 pF on other signals.

Table 12-20. SDRAM Clock Signal.

| Symbol                   | Parameter                        | Max <sup>(1)</sup>      | Units |
|--------------------------|----------------------------------|-------------------------|-------|
| 1/(t <sub>CPSDCK</sub> ) | SDRAM Controller Clock Frequency | 1/(t <sub>cpcpu</sub> ) | MHz   |

Note: 1. The maximum frequency of the SDRAMC interface is the same as the max frequency for the HSB.

Table 12-21. SDRAM Clock Signal.

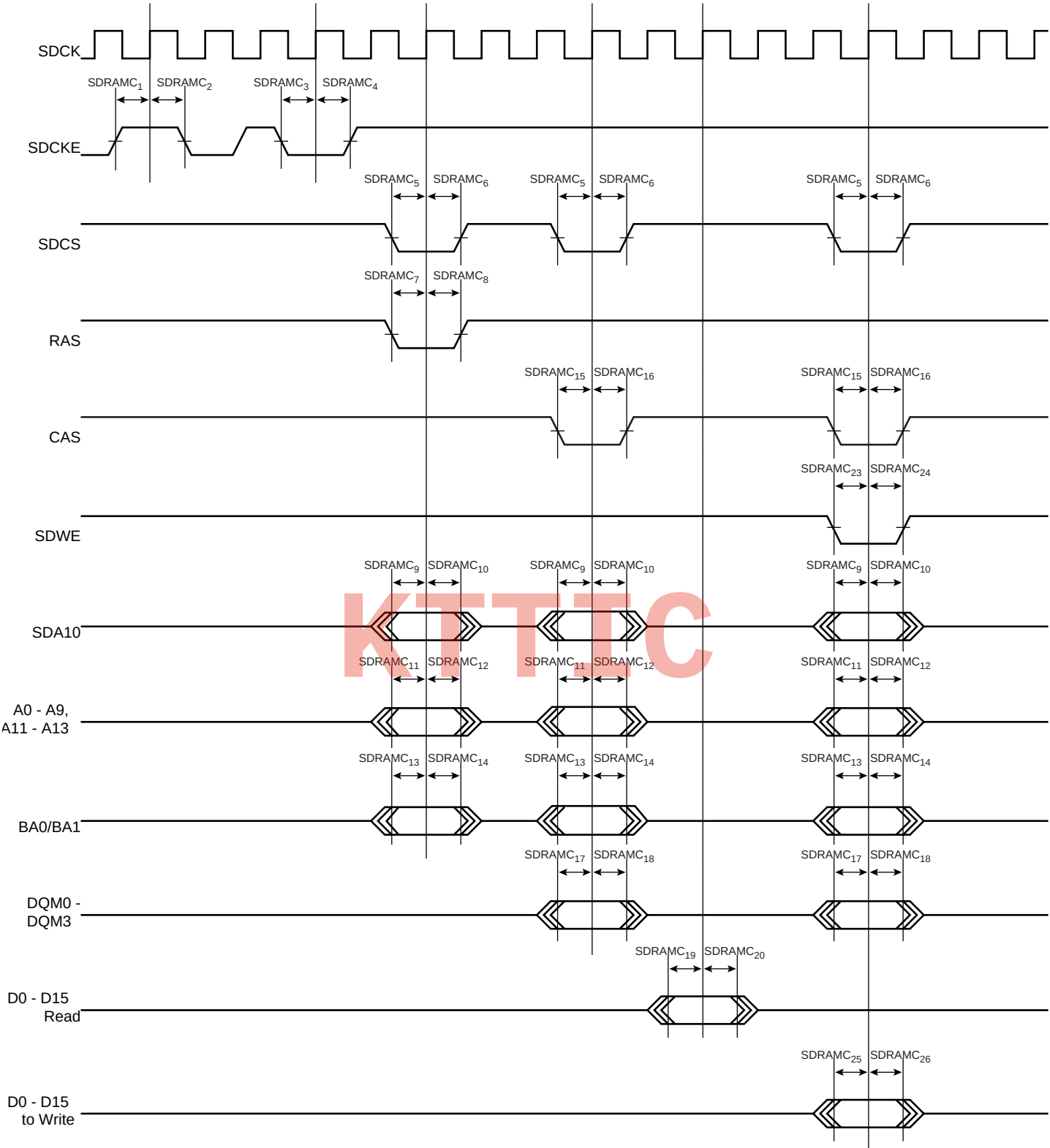
| Symbol               | Parameter                            | Min | Units |
|----------------------|--------------------------------------|-----|-------|
| SDRAMC <sub>1</sub>  | SDCKE High before SDCK Rising Edge   | 7.4 | ns    |
| SDRAMC <sub>2</sub>  | SDCKE Low after SDCK Rising Edge     | 3.2 |       |
| SDRAMC <sub>3</sub>  | SDCKE Low before SDCK Rising Edge    | 7   |       |
| SDRAMC <sub>4</sub>  | SDCKE High after SDCK Rising Edge    | 2.9 |       |
| SDRAMC <sub>5</sub>  | SDCS Low before SDCK Rising Edge     | 7.5 |       |
| SDRAMC <sub>6</sub>  | SDCS High after SDCK Rising Edge     | 1.6 |       |
| SDRAMC <sub>7</sub>  | RAS Low before SDCK Rising Edge      | 7.2 |       |
| SDRAMC <sub>8</sub>  | RAS High after SDCK Rising Edge      | 2.3 |       |
| SDRAMC <sub>9</sub>  | SDA10 Change before SDCK Rising Edge | 7.6 |       |
| SDRAMC <sub>10</sub> | SDA10 Change after SDCK Rising Edge  | 1.9 |       |

Table 12-21. SDRAM Clock Signal.

| Symbol               | Parameter                                | Min | Units |
|----------------------|------------------------------------------|-----|-------|
| SDRAMC <sub>11</sub> | Address Change before SDCK Rising Edge   | 6.2 | ns    |
| SDRAMC <sub>12</sub> | Address Change after SDCK Rising Edge    | 2.2 |       |
| SDRAMC <sub>13</sub> | Bank Change before SDCK Rising Edge      | 6.3 |       |
| SDRAMC <sub>14</sub> | Bank Change after SDCK Rising Edge       | 2.4 |       |
| SDRAMC <sub>15</sub> | CAS Low before SDCK Rising Edge          | 7.4 |       |
| SDRAMC <sub>16</sub> | CAS High after SDCK Rising Edge          | 1.9 |       |
| SDRAMC <sub>17</sub> | DQM Change before SDCK Rising Edge       | 6.4 |       |
| SDRAMC <sub>18</sub> | DQM Change after SDCK Rising Edge        | 2.2 |       |
| SDRAMC <sub>19</sub> | D0-D15 in Setup before SDCK Rising Edge  | 9   |       |
| SDRAMC <sub>20</sub> | D0-D15 in Hold after SDCK Rising Edge    | 0   |       |
| SDRAMC <sub>23</sub> | SDWE Low before SDCK Rising Edge         | 7.6 |       |
| SDRAMC <sub>24</sub> | SDWE High after SDCK Rising Edge         | 1.8 |       |
| SDRAMC <sub>25</sub> | D0-D15 Out Valid before SDCK Rising Edge | 7.1 |       |
| SDRAMC <sub>26</sub> | D0-D15 Out Valid after SDCK Rising Edge  | 1.5 |       |

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Figure 12-4. SDRAMC Signals relative to SDCK.



12.10 JTAG Timings

12.10.1 JTAG Interface Signals

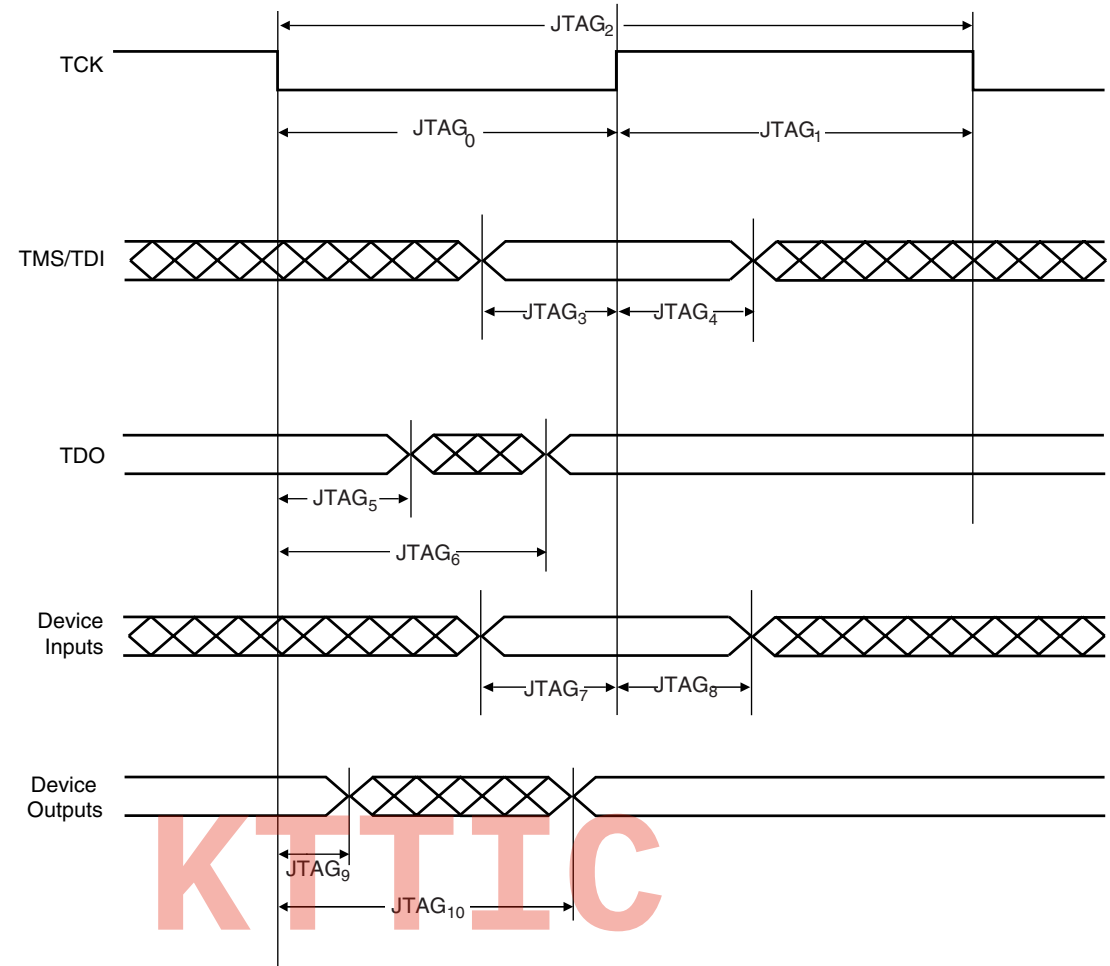
Table 12-22. JTAG Interface Timing specification

| Symbol             | Parameter                      | Conditions | Min | Max | Units |
|--------------------|--------------------------------|------------|-----|-----|-------|
| JTAG <sub>0</sub>  | TCK Low Half-period            | (1)        | 6   |     | ns    |
| JTAG <sub>1</sub>  | TCK High Half-period           | (1)        | 3   |     | ns    |
| JTAG <sub>2</sub>  | TCK Period                     | (1)        | 9   |     | ns    |
| JTAG <sub>3</sub>  | TDI, TMS Setup before TCK High | (1)        | 1   |     | ns    |
| JTAG <sub>4</sub>  | TDI, TMS Hold after TCK High   | (1)        | 0   |     | ns    |
| JTAG <sub>5</sub>  | TDO Hold Time                  | (1)        | 4   |     | ns    |
| JTAG <sub>6</sub>  | TCK Low to TDO Valid           | (1)        |     | 6   | ns    |
| JTAG <sub>7</sub>  | Device Inputs Setup Time       | (1)        |     |     | ns    |
| JTAG <sub>8</sub>  | Device Inputs Hold Time        | (1)        |     |     | ns    |
| JTAG <sub>9</sub>  | Device Outputs Hold Time       | (1)        |     |     | ns    |
| JTAG <sub>10</sub> | TCK to Device Outputs Valid    | (1)        |     |     | ns    |

Note: 1. V<sub>VDDIO</sub> from 3.0V to 3.6V, maximum external capacitor = 40pF

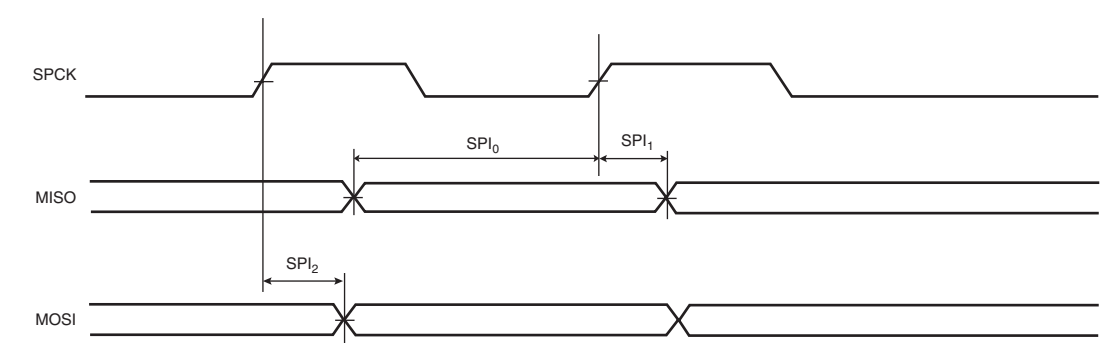
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Figure 12-5. JTAG Interface Signals

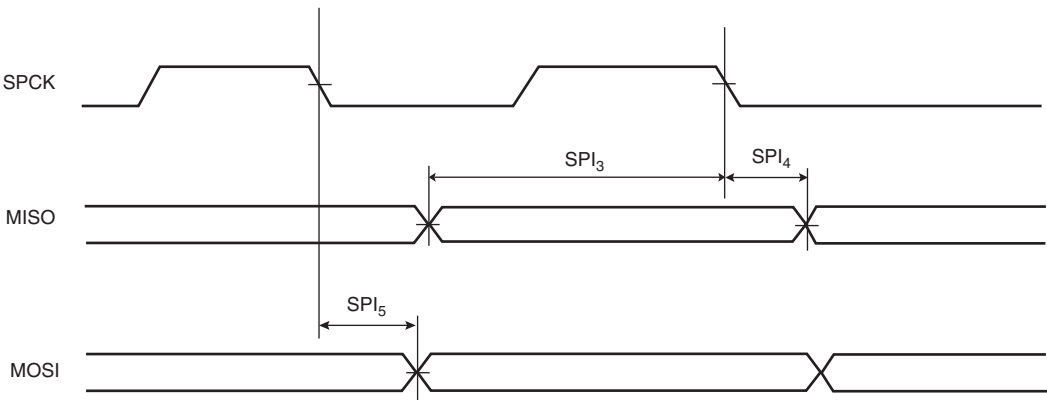


12.11 SPI Characteristics

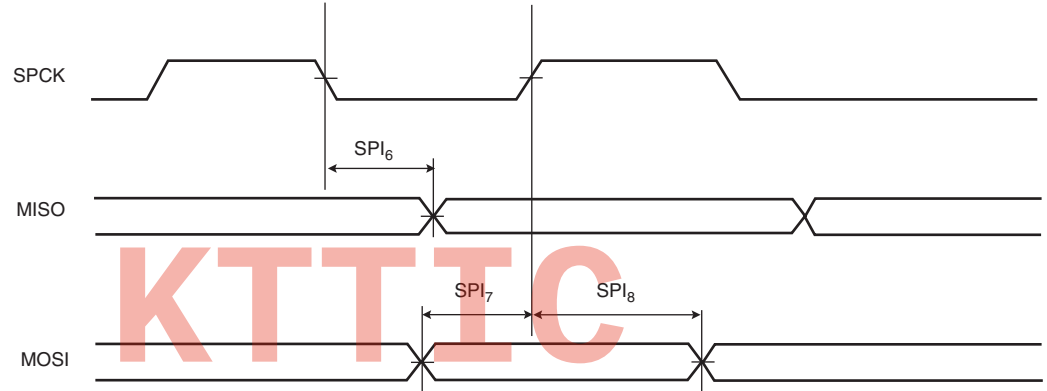
Figure 12-6. SPI Master mode with (CPOL = NCPHA = 0) or (CPOL= NCPHA= 1)



**Figure 12-7.** SPI Master mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)



**Figure 12-8.** SPI Slave mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)



**Figure 12-9.** SPI Slave mode with (CPOL = NCPHA = 0) or (CPOL= NCPHA= 1)

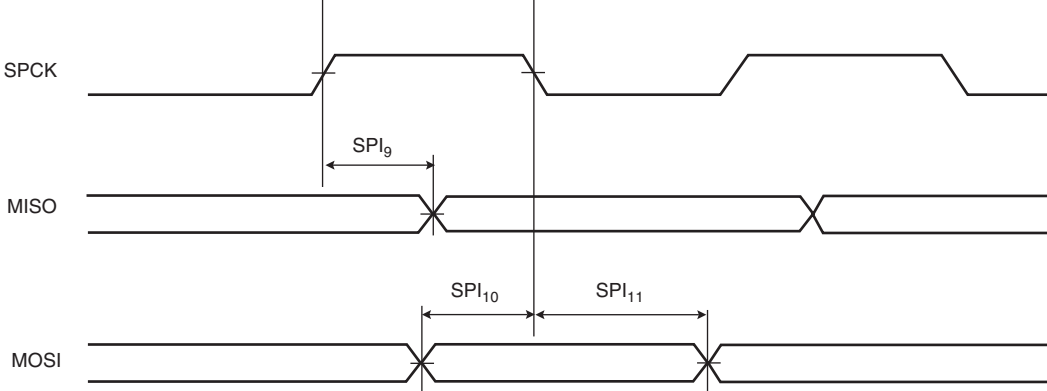


Table 12-23. SPI Timings

| Symbol            | Parameter                                  | Conditions                 | Min                        | Max  | Units |
|-------------------|--------------------------------------------|----------------------------|----------------------------|------|-------|
| SPI <sub>0</sub>  | MISO Setup time before SPCK rises (master) | 3.3V domain <sup>(1)</sup> | $22 + (t_{CPMCK})/2^{(2)}$ |      | ns    |
| SPI <sub>1</sub>  | MISO Hold time after SPCK rises (master)   | 3.3V domain <sup>(1)</sup> | 0                          |      | ns    |
| SPI <sub>2</sub>  | SPCK rising to MOSI Delay (master)         | 3.3V domain <sup>(1)</sup> |                            | 7    | ns    |
| SPI <sub>3</sub>  | MISO Setup time before SPCK falls (master) | 3.3V domain <sup>(1)</sup> | $22 + (t_{CPMCK})/2^{(2)}$ |      | ns    |
| SPI <sub>4</sub>  | MISO Hold time after SPCK falls (master)   | 3.3V domain <sup>(1)</sup> | 0                          |      | ns    |
| SPI <sub>5</sub>  | SPCK falling to MOSI Delay (master)        | 3.3V domain <sup>(1)</sup> |                            | 7    | ns    |
| SPI <sub>6</sub>  | SPCK falling to MISO Delay (slave)         | 3.3V domain <sup>(1)</sup> |                            | 26.5 | ns    |
| SPI <sub>7</sub>  | MOSI Setup time before SPCK rises (slave)  | 3.3V domain <sup>(1)</sup> | 0                          |      | ns    |
| SPI <sub>8</sub>  | MOSI Hold time after SPCK rises (slave)    | 3.3V domain <sup>(1)</sup> | 1.5                        |      | ns    |
| SPI <sub>9</sub>  | SPCK rising to MISO Delay (slave)          | 3.3V domain <sup>(1)</sup> |                            | 27   | ns    |
| SPI <sub>10</sub> | MOSI Setup time before SPCK falls (slave)  | 3.3V domain <sup>(1)</sup> | 0                          |      | ns    |
| SPI <sub>11</sub> | MOSI Hold time after SPCK falls (slave)    | 3.3V domain <sup>(1)</sup> | 1                          |      | ns    |

Notes: 1. 3.3V domain: V<sub>VDDIO</sub> from 3.0V to 3.6V, maximum external capacitor = 40 pF.

2. t<sub>CPMCK</sub>: Master Clock period in ns.

## 12.12 MACB Characteristics

Table 12-24. Ethernet MAC Signals

| Symbol            | Parameter                        | Conditions                | Min (ns) | Max (ns) |
|-------------------|----------------------------------|---------------------------|----------|----------|
| EMAC <sub>1</sub> | Setup for EMDIO from EMDC rising | Load: 20pF <sup>(2)</sup> |          |          |
| EMAC <sub>2</sub> | Hold for EMDIO from EMDC rising  | Load: 20pF <sup>(2)</sup> |          |          |
| EMAC <sub>3</sub> | EMDIO toggling from EMDC falling | Load: 20pF <sup>(2)</sup> |          |          |

Notes: 1. f: MCK frequency (MHz)

2. V<sub>VDDIO</sub> from 3.0V to 3.6V, maximum external capacitor = 20 pF

Table 12-25. Ethernet MAC MII Specific Signals

| Symbol             | Parameter                        | Conditions                | Min (ns) | Max (ns) |
|--------------------|----------------------------------|---------------------------|----------|----------|
| EMAC <sub>4</sub>  | Setup for ECOL from ETXCK rising | Load: 20pF <sup>(1)</sup> | 3        |          |
| EMAC <sub>5</sub>  | Hold for ECOL from ETXCK rising  | Load: 20pF <sup>(1)</sup> | 0        |          |
| EMAC <sub>6</sub>  | Setup for ECRS from ETXCK rising | Load: 20pF <sup>(1)</sup> | 3        |          |
| EMAC <sub>7</sub>  | Hold for ECRS from ETXCK rising  | Load: 20pF <sup>(1)</sup> | 0        |          |
| EMAC <sub>8</sub>  | ETXER toggling from ETXCK rising | Load: 20pF <sup>(1)</sup> |          | 15       |
| EMAC <sub>9</sub>  | ETXEN toggling from ETXCK rising | Load: 20pF <sup>(1)</sup> |          | 15       |
| EMAC <sub>10</sub> | ETX toggling from ETXCK rising   | Load: 20pF <sup>(1)</sup> |          | 15       |
| EMAC <sub>11</sub> | Setup for ERX from ERXCK         | Load: 20pF <sup>(1)</sup> | 1        |          |



Table 12-25. Ethernet MAC MII Specific Signals

| Symbol             | Parameter                  | Conditions                | Min (ns) | Max (ns) |
|--------------------|----------------------------|---------------------------|----------|----------|
| EMAC <sub>12</sub> | Hold for ERX from ERXCK    | Load: 20pF <sup>(1)</sup> | 1.5      |          |
| EMAC <sub>13</sub> | Setup for ERXER from ERXCK | Load: 20pF <sup>(1)</sup> | 1        |          |
| EMAC <sub>14</sub> | Hold for ERXER from ERXCK  | Load: 20pF <sup>(1)</sup> | 0.5      |          |
| EMAC <sub>15</sub> | Setup for ERXDV from ERXCK | Load: 20pF <sup>(1)</sup> | 1.5      |          |
| EMAC <sub>16</sub> | Hold for ERXDV from ERXCK  | Load: 20pF <sup>(1)</sup> | 1        |          |

Note: 1. V<sub>VDDIO</sub> from 3.0V to 3.6V, maximum external capacitor = 20 pF

Figure 12-10. Ethernet MAC MII Mode

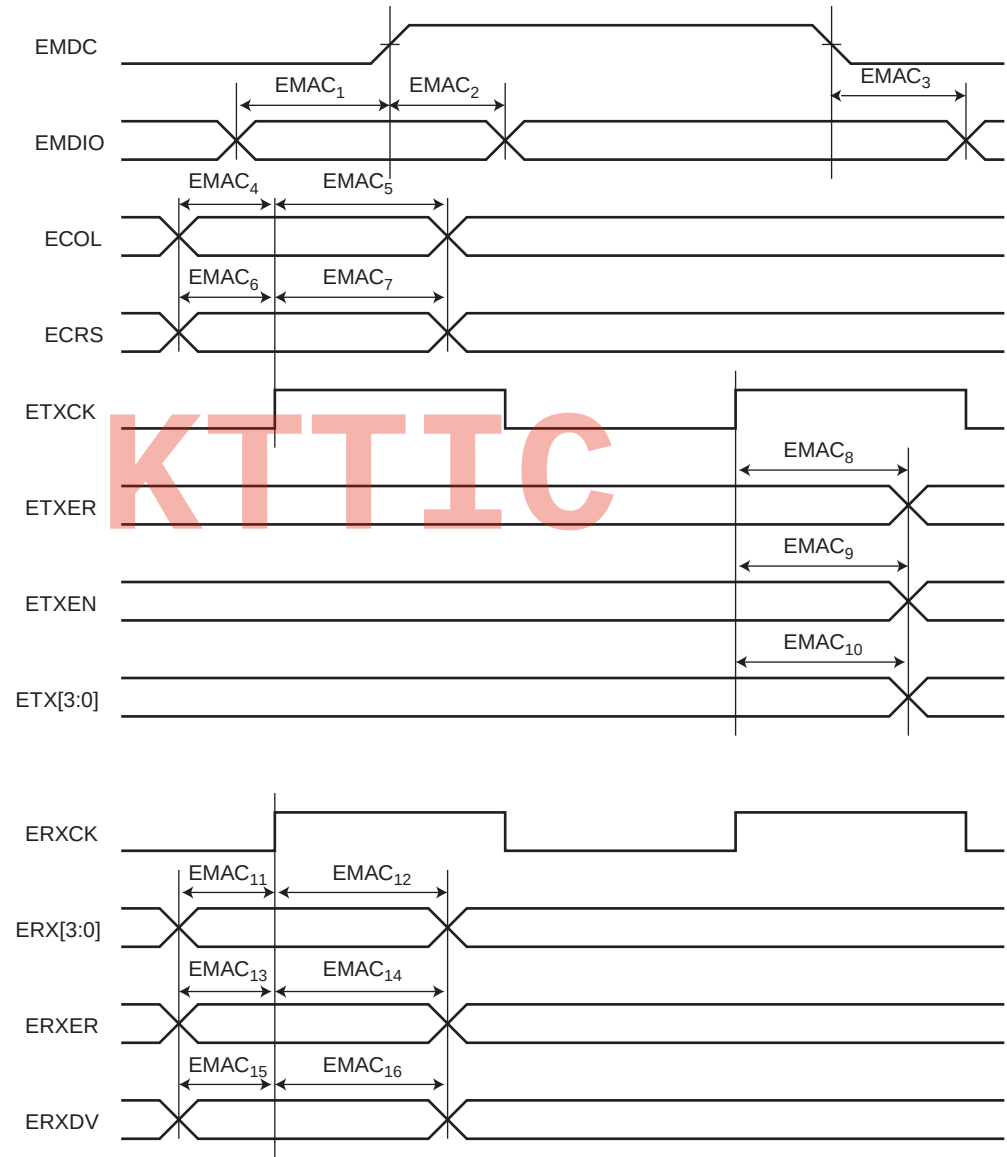
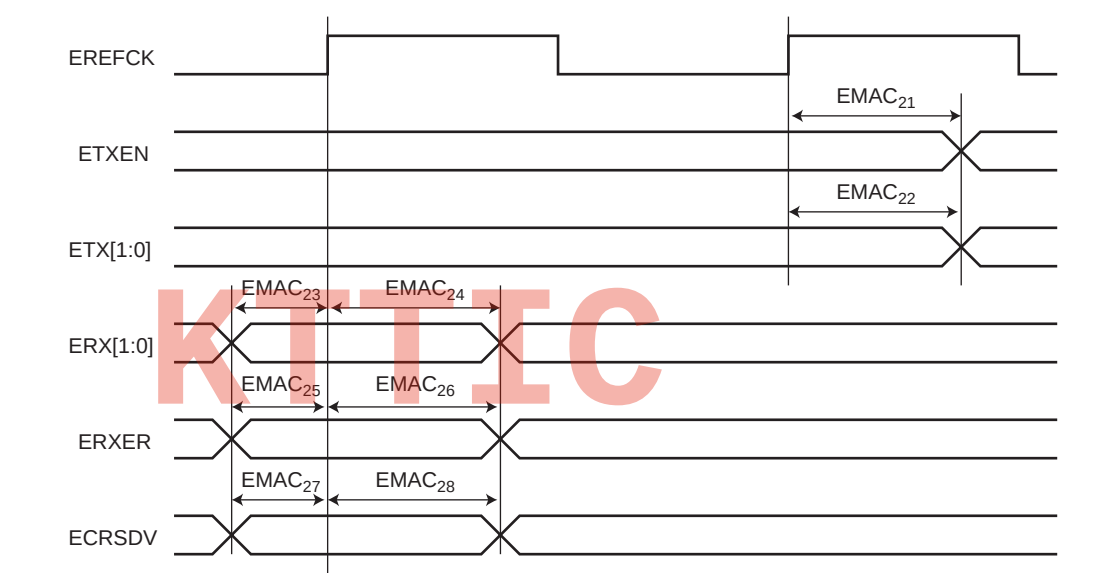


Table 12-26. Ethernet MAC RMII Specific Signals

| Symbol             | Parameter                         | Min (ns) | Max (ns) |
|--------------------|-----------------------------------|----------|----------|
| EMAC <sub>21</sub> | ETXEN toggling from EREFCK rising | 7        | 14.5     |
| EMAC <sub>22</sub> | ETX toggling from EREFCK rising   | 7        | 14.7     |
| EMAC <sub>23</sub> | Setup for ERX from EREFCK         | 1.5      |          |
| EMAC <sub>24</sub> | Hold for ERX from EREFCK          | 0        |          |
| EMAC <sub>25</sub> | Setup for ERXER from EREFCK       | 1.5      |          |
| EMAC <sub>26</sub> | Hold for ERXER from EREFCK        | 0        |          |
| EMAC <sub>27</sub> | Setup for ECRSDV from EREFCK      | 1.5      |          |
| EMAC <sub>28</sub> | Hold for ECRSDV from EREFCK       | 0        |          |

Figure 12-11. Ethernet MAC RMII Mode



12.13 Flash Characteristics

The following table gives the device maximum operating frequency depending on the field FWS of the Flash FSR register. This field defines the number of wait states required to access the Flash Memory.

Table 12-27. Flash Wait States

| FWS | Read Operations | Maximum Operating Frequency (MHz) |
|-----|-----------------|-----------------------------------|
| 0   | 1 cycle         | 33                                |
| 1   | 2 cycles        | 66                                |

## 13. Mechanical Characteristics

### 13.1 Thermal Considerations

#### 13.1.1 Thermal Data

Table 13-1 summarizes the thermal resistance data depending on the package.

**Table 13-1.** Thermal Resistance Data

| Symbol        | Parameter                              | Condition | Package | Typ | Unit |
|---------------|----------------------------------------|-----------|---------|-----|------|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | Still Air | TQFP100 | TBD | °C/W |
| $\theta_{JC}$ | Junction-to-case thermal resistance    |           | TQFP100 | TBD |      |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | Still Air | LQFP144 | TBD | °C/W |
| $\theta_{JC}$ | Junction-to-case thermal resistance    |           | LQFP144 | TBD |      |

#### 13.1.2 Junction Temperature

The average chip-junction temperature,  $T_J$ , in °C can be obtained from the following:

1.  $T_J = T_A + (P_D \times \theta_{JA})$
2.  $T_J = T_A + (P_D \times (\theta_{HEAT SINK} + \theta_{JC}))$

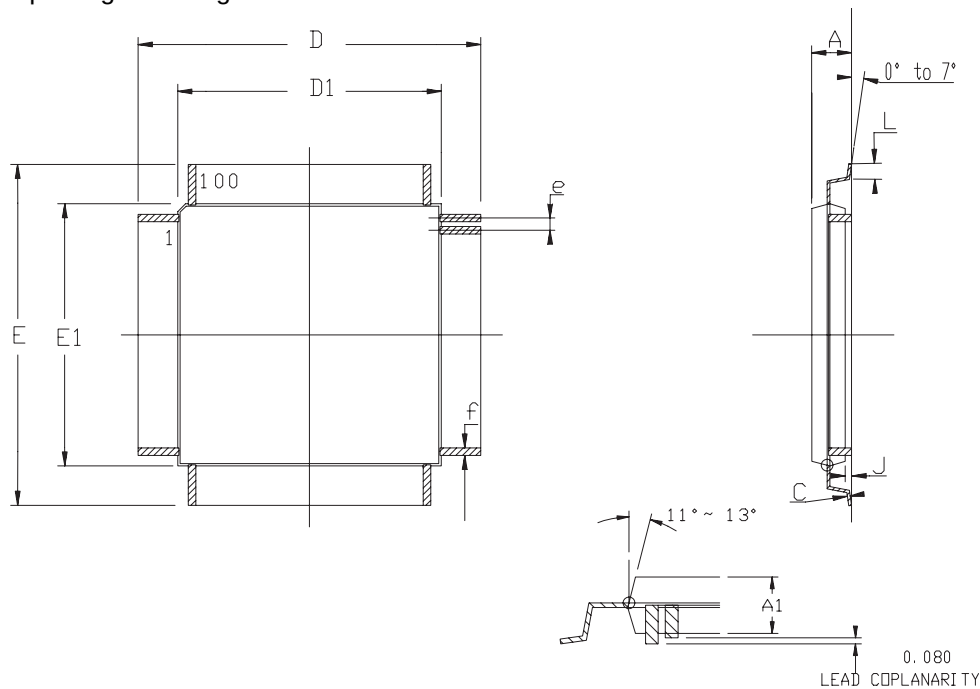
where:

- $\theta_{JA}$  = package thermal resistance, Junction-to-ambient (°C/W), provided in [Table 13-1 on page 59](#).
- $\theta_{JC}$  = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in [Table 13-1 on page 59](#).
- $\theta_{HEAT SINK}$  = cooling device thermal resistance (°C/W), provided in the device datasheet.
- $P_D$  = device power consumption (W) estimated from data provided in the section "[Power Consumption](#)" on page 42.
- $T_A$  = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature  $T_J$  in °C.

13.2 Package Drawings

Figure 13-1. TQFP-100 package drawing



|    | MM        |      | INCH     |      |
|----|-----------|------|----------|------|
|    | Min       | Max  | Min      | Max  |
| A  | ---       | 1.20 | ---      | .047 |
| A1 | 0.95      | 1.05 | .037     | .041 |
| C  | 0.09      | 0.20 | .004     | .008 |
| D  | 16.00 BSC |      | .630 BSC |      |
| D1 | 14.00 BSC |      | .551 BSC |      |
| E  | 16.00 BSC |      | .630 BSC |      |
| E1 | 14.00 BSC |      | .551 BSC |      |
| J  | 0.05      | 0.15 | .002     | .006 |
| L  | 0.45      | 0.75 | .018     | .030 |
| e  | 0.50 BSC  |      | .020 BSC |      |
| f  | 0.17      | 0.27 | .007     | .011 |

Table 13-2. Device and Package Maximum Weight

|     |    |
|-----|----|
| TBD | mg |
|-----|----|

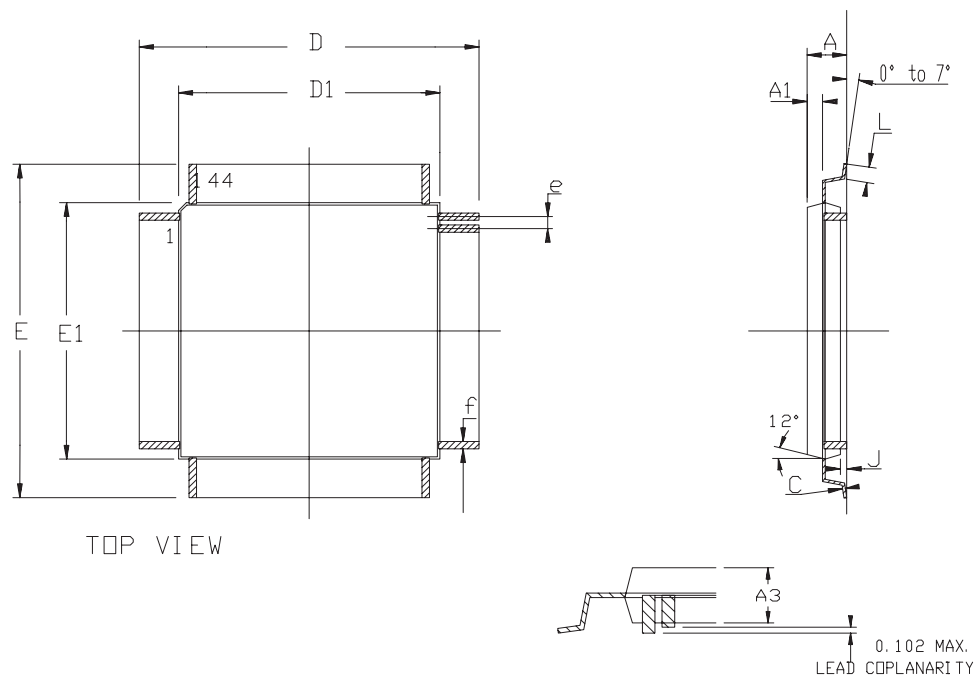
Table 13-3. Package Characteristics

|                            |     |
|----------------------------|-----|
| Moisture Sensitivity Level | TBD |
|----------------------------|-----|

Table 13-4. Package Reference

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification   | E3     |

Figure 13-2. LQFP-144 package drawing



|    | MM       |       | INCH      |      |
|----|----------|-------|-----------|------|
|    | Min      | Max   | Min       | Max  |
| A  | -        | 1.60  | -         | .063 |
| C  | 0.09     | 0.20  | .004      | .008 |
| A3 | 1.35     | 1.45  | .053      | .057 |
| D  | 21.90    | 22.10 | .862      | .870 |
| D1 | 19.90    | 20.10 | .783      | .791 |
| E  | 21.90    | 22.10 | .862      | .870 |
| E1 | 19.90    | 20.10 | .783      | .791 |
| J  | 0.05     | 0.15  | .002      | .006 |
| L  | 0.45     | 0.75  | .018      | .030 |
| e  | 0.50 BSC |       | .0197 BSC |      |
| f  | 0.22 BSC |       | .009 BSC  |      |

Table 13-5. Device and Package Maximum Weight

|     |    |
|-----|----|
| TBD | mg |
|-----|----|

Table 13-6. Package Characteristics

|                            |     |
|----------------------------|-----|
| Moisture Sensitivity Level | TBD |
|----------------------------|-----|

Table 13-7. Package Reference

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification   | E3     |

13.3 Soldering Profile

Table 13-8 gives the recommended soldering profile from J-STD-20.

Table 13-8. Soldering Profile

| Profile Feature                            | Green Package |
|--------------------------------------------|---------------|
| Average Ramp-up Rate (217°C to Peak)       | TBD           |
| Preheat Temperature 175°C ±25°C            | TBD           |
| Temperature Maintained Above 217°C         | TBD           |
| Time within 5°C of Actual Peak Temperature | TBD           |
| Peak Temperature Range                     | TBD           |
| Ramp-down Rate                             | TBD           |
| Time 25°C to Peak Temperature              | TBD           |

Note: It is recommended to apply a soldering temperature higher than 250°C.  
A maximum of three reflow passes is allowed per component.

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14. Ordering Information

Table 14-1. Ordering Information

| Device       | Ordering Code      | Package       | Conditioning | Temperature Operating Range           |
|--------------|--------------------|---------------|--------------|---------------------------------------|
| AT32UC3A0512 | AT32UC3A0512-ALUT  | 144 lead LQFP | Tray         | Industrial (-40°C to 85°C)            |
|              | AT32UC3A0512-ALTR  | 144 lead LQFP | Reels        | Automotive (-40°C to 85°C)            |
|              | AT32UC3A0512-ALTT  | 144 lead LQFP | Tray         | Automotive (-40°C to 85°C)            |
|              | AT32UC3A0512-ALTES | 144 lead LQFP | Tray         | Automotive (-40°C to 85°C)<br>samples |
| AT32UC3A0256 | AT32UC3A0256-ALUT  | 144 lead LQFP | Tray         | Industrial (-40°C to 85°C)            |
| AT32UC3A0128 | AT32UC3A0128-ALUT  | 144 lead LQFP | Tray         | Industrial (-40°C to 85°C)            |
| AT32UC3A1512 | AT32UC3A1512-AUT   | 100 lead TQFP | Tray         | Industrial (-40°C to 85°C)            |
| AT32UC3A1256 | AT32UC3A1256-AUT   | 100 lead TQFP | Tray         | Industrial (-40°C to 85°C)            |
| AT32UC3A1128 | AT32UC3A1128-AUT   | 100 lead TQFP | Tray         | Industrial (-40°C to 85°C)            |

14.1 Automotive Quality Grade

The AT32UC3A have been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949. This data sheet will contain limit values extracted from the results of extensive characterization (Temperature and Voltage). The quality and reliability of the AT32UC3A is verified during regular product qualification as per AEC-Q100 grade 3.

As indicated in the ordering information paragraph, the product is available in only one temperature grade T: -40°C / + 85°C.



## 15. Errata

All industrial parts labelled with -UES (engineering samples) are revision E parts.

### 15.1 Rev. I

#### 15.1.1 PWM

**1. PWM channel interrupt enabling triggers an interrupt**

When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

**Fix/Workaround**

When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

**2. PWN counter restarts at 0x0001**

The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

**Fix/Workaround**

- The first period is 0x0000, 0x0001, ..., period
- Consecutive periods are 0x0001, 0x0002, ..., period

**3. PWM update period to a 0 value does not work**

It is impossible to update a period equal to 0 by the using the PWM update register (PWM\_CUPD).

**Fix/Workaround**

Do not update the PWM\_CUPD register with a value equal to 0.

#### 15.1.2 ADC

**1. ADC possible miss on DRDY when disabling a channel**

The ADC does not work properly when more than one channel is enabled.

**Fix/Workaround**

Do not use the ADC with more than one channel enabled at a time.

**2. Sleep Mode activation needs additionnal A to D conversion**

If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

**Fix/Workaround**

Activate the sleep mode in the mode register and then perform an AD conversion.

#### 15.1.3 SPI

**1. SPI Slave / PDCA transfer: no TX UNDERRUN flag**

There is no TX UNDERRUN flag available, therefore in SPI slave mode, there is no way to be informed of a character lost in transmission.

**Fix/Workaround**

For PDCA transfer: none.



**2. SPI FDIV option does not work**

Selecting clock signal using FDIV = 1 does not work as specified.

**Fix/Workaround**

Do not set FDIV = 1.

**3. SPI Bad Serial Clock Generation on 2nd chip\_select when SCBR = 1, CPOL=1 and NCPHA=0**

When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.

**Fix/workaround**

When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

**4. SPI Glitch on RXREADY flag in slave mode when enabling the SPI or during the first transfer**

In slave mode, the SPI can generate a false RXREADY signal during enabling of the SPI or during the first transfer.

**Fix/Workaround**

1. Set slave mode, set required CPOL/CPHA.
2. Enable SPI.
3. Set the polarity CPOL of the line in the opposite value of the required one.
4. Set the polarity CPOL to the required one.
5. Read the RXHOLDING register.

Transfers can now begin and RXREADY will now behave as expected.

**15.1.4 Power Manager**

**1. If the BOD level is higher than VDDCORE, the part is constantly resetted**

If the BOD level is set to a value higher than VDDCORE and enabled by fuses, the part will be in constant reset.

**Fix/Workaround**

Apply an external voltage on VDDCORE that is higher than the BOD level and is lower than VDDCORE max and disable the BOD.

**15.1.5 Flashc**

**1. On AT32UC3A0512 and AT32UC3A1512, corrupted read in flash after FLASHC WP, EP, EA, WUP, EUP commands may happen**

- After a FLASHC Write Page (WP) or Erase Page (EP) command applied to a page in a given half of the flash (first or last 256 kB of flash), reading (data read or code fetch) the other half of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

- After a FLASHC Erase All (EA) command, reading (data read or code fetch) the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

- After a FLASHC Write User Page (WUP) or Erase User Page (EUP) command, reading (data read or code fetch) the second half (last 256 kB) of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

**Fix/Workaround**

Flashc WP, EP, EA, WUP, EUP commands: these commands must be issued from RAM or through the EBI. After these commands, read twice one flash page initialized to 00h in each half part of the flash.

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## 15.2 Rev. H

### 15.2.1 PWM

#### 1. PWM channel interrupt enabling triggers an interrupt

When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

##### Fix/Workaround

When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

#### 2. PWN counter restarts at 0x0001

The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

##### Fix/Workaround

- The first period is 0x0000, 0x0001, ..., period
- Consecutive periods are 0x0001, 0x0002, ..., period

#### 3. PWM update period to a 0 value does not work

It is impossible to update a period equal to 0 by the using the PWM update register (PWM\_CUPD).

##### Fix/Workaround

Do not update the PWM\_CUPD register with a value equal to 0.

### 15.2.2 ADC

#### 1. ADC possible miss on DRDY when disabling a channel

The ADC does not work properly when more than one channel is enabled.

##### Fix/Workaround

Do not use the ADC with more than one channel enabled at a time.

#### 2. Sleep Mode activation needs additionnal A to D conversion

If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

##### Fix/Workaround

Activate the sleep mode in the mode register and then perform an AD conversion.

### 15.2.3 SPI

#### 1. SPI Slave / PDCA transfer: no TX UNDERRUN flag

There is no TX UNDERRUN flag available, therefore in SPI slave mode, there is no way to be informed of a character lost in transmission.

##### Fix/Workaround

For PDCA transfer: none.

#### 2. SPI FDIV option does not work

Selecting clock signal using FDIV = 1 does not work as specified.

##### Fix/Workaround

Do not set FDIV = 1

**3. SPI disable does not work in SLAVE mode.**

**Fix/Workaround**

Read the last received data, then perform a Software Reset.

**4. SPI Bad Serial Clock Generation on 2nd chip\_select when SCBR = 1, CPOL=1 and NCPHA=0**

When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.

**Fix/workaround**

When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

**5. SPI Glitch on RXREADY flag in slave mode when enabling the SPI or during the first transfer**

In slave mode, the SPI can generate a false RXREADY signal during enabling of the SPI or during the first transfer.

**Fix/Workaround**

1. Set slave mode, set required CPOL/CPHA.
2. Enable SPI.
3. Set the polarity CPOL of the line in the opposite value of the required one.
4. Set the polarity CPOL to the required one.
5. Read the RXHOLDING register.

Transfers can now begin and RXREADY will now behave as expected.

## 15.2.4 Power Manager

**1. Wrong reset causes when BOD is activated**

Setting the BOD enable fuse will cause the Reset Cause Register to list BOD reset as the reset source even though the part was reset by another source.

**Fix/Workaround**

Do not set the BOD enable fuse, but activate the BOD as soon as your program starts.

**2. If the BOD level is higher than VDDCORE, the part is constantly reset**

If the BOD level is set to a value higher than VDDCORE and enabled by fuses, the part will be in constant reset.

**Fix/Workaround**

Apply an external voltage on VDDCORE that is higher than the BOD level and is lower than VDDCORE max and disable the BOD.

## 15.2.5 FLASHC

**1. On AT32UC3A0512 and AT32UC3A1512, corrupted read in flash after FLASHC WP, EP, EA, WUP, EUP commands may happen**

- After a FLASHC Write Page (WP) or Erase Page (EP) command applied to a page in a given half of the flash (first or last 256 kB of flash), reading (data read or code fetch) the other half of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

- After a FLASHC Erase All (EA) command, reading (data read or code fetch) the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

- After a FLASHC Write User Page (WUP) or Erase User Page (EUP) command, reading (data read or code fetch) the second half (last 256 kB) of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

**Fix/Workaround**

Flashc WP, EP, EA, WUP, EUP commands: these commands must be issued from RAM or through the EBI. After these commands, read twice one flash page initialized to 00h in each half part of the flash.

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## 15.3 Rev. E

### 15.3.1 SPI

**1. SPI FDIV option does not work**

Selecting clock signal using FDIV = 1 does not work as specified.

**Fix/Workaround**

Do not set FDIV = 1.

**2. SPI Slave / PDCA transfer: no TX UNDERRUN flag**

There is no TX UNDERRUN flag available, therefore in SPI slave mode, there is no way to be informed of a character lost in transmission.

**Fix/Workaround**

For PDCA transfer: none.

**3. SPI Bad serial clock generation on 2nd chip select when SCBR=1, CPOL=1 and CNCPHA=0**

When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.

**Fix/Workaround**

When multiple CS are in use, if one of the baudrate equals to 1, the other must also equal 1 if CPOL=1 and CPHA=0.

**4. SPI Glitch on RXREADY flag in slave mode when enabling the SPI or during the first transfer**

In slave mode, the SPI can generate a false RXREADY signal during enabling of the SPI or during the first transfer.

**Fix/Workaround**

1. Set slave mode, set required CPOL/CPHA.
2. Enable SPI.
3. Set the polarity CPOL of the line in the opposite value of the required one.
4. Set the polarity CPOL to the required one.
5. Read the RXHOLDING register.

Transfers can now begin and RXREADY will now behave as expected.

**5. SPI CSNAAT bit 2 in register CSR0...CSR3 is not available.**

**Fix/Workaround**

Do not use this bit.

**6. SPI disable does not work in SLAVE mode.**

**Fix/Workaround**

Read the last received data, then perform a Software Reset.

**7. SPI Bad Serial Clock Generation on 2nd chip\_select when SCBR = 1, CPOL=1 and NCPHA=0**

When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.

**Fix/workaround**

When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

**15.3.2 PWM****1. PWM counter restarts at 0x0001**

The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

**Fix/Workaround**

- The first period is 0x0000, 0x0001, ..., period
- Consecutive periods are 0x0001, 0x0002, ..., period

**2. PWM channel interrupt enabling triggers an interrupt**

When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

**Fix/Workaround**

When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

**3. PWM update period to a 0 value does not work**

It is impossible to update a period equal to 0 by the using the PWM update register (PWM\_CUPD).

**Fix/Workaround**

Do not update the PWM\_CUPD register with a value equal to 0.

**4. PWM channel status may be wrong if disabled before a period has elapsed**

Before a PWM period has elapsed, the read channel status may be wrong. The CHIDx-bit for a PWM channel in the PWM Enable Register will read '1' for one full PWM period even if the channel was disabled before the period elapsed. It will then read '0' as expected.

**Fix/Workaround**

Reading the PWM channel status of a disabled channel is only correct after a PWM period has elapsed.

**15.3.3 SSC****1. SSC does not trigger RF when data is low**

The SSC cannot transmit or receive data when CKS = CKDIV and CKO = none, in TCMR or RCMR respectively.

**Fix/Workaround**

Set CKO to a value that is not "none" and bypass the output of the TK/RK pin with the PIO.

**2. SSC Data is not sent unless clock is set as output**

The SSC cannot transmit or receive data when CKS = CKDIV and CKO = none, in TCMR or RCMR respectively.

**Fix/Workaround**

Set CKO to a value that is not "none" and bypass the output of the TK/RK pin with the PIO.

#### 15.3.4 USB

##### 1. USB No end of host reset signaled upon disconnection

In host mode, in case of an unexpected device disconnection whereas a usb reset is being sent by the usb controller, the UHCON.RESET bit may not be cleared by the hardware at the end of the reset.

###### Fix/Workaround

A software workaround consists in testing (by polling or interrupt) the disconnection (UHINT.DDISCI == 1) while waiting for the end of reset (UHCON.RESET == 0) to avoid being stuck.

##### 2. USBFSM and UHADDR1/2/3 registers are not available.

Do not use USBFSM register.

###### Fix/Workaround

Do not use USBFSM register and use HCON[6:0] field instead for all the pipes.

#### 15.3.5 Processor and Architecture

##### 1. Incorrect Processor ID

The processor ID reads 0x01 and not 0x02 as it should.

###### Fix/Workaround

None.

##### 2. Bus error should be masked in Debug mode

If a bus error occurs during debug mode, the processor will not respond to debug commands through the DINST register.

###### Fix/Workaround

A reset of the device will make the CPU respond to debug commands again.

##### 3. Read Modify Write (RMW) instructions on data outside the internal RAM does not work.

Read Modify Write (RMW) instructions on data outside the internal RAM does not work.

###### Fix/Workaround

Do not perform RMW instructions on data outside the internal RAM.

##### 4. CRC calculation of a locked device will calculate CRC for 512 kB of flash memory, even though the part has less flash.

###### Fix/Workaround

The flash address space is wrapping, so it is possible to use the CRC value by calculating CRC of the flash content concatenated with itself N times. Where N is 512 kB/flash size.

##### 5. Need two NOPs instruction after instructions masking interrupts

The instructions following in the pipeline the instruction masking the interrupt through SR may behave abnormally.

###### Fix/Workaround

Place two NOPs instructions after each SSRF or MTSR instruction setting IxM or GM in SR.



6. **CPU Cycle Counter does not reset the COUNT system register on COMPARE match.**  
The device revision E does not reset the COUNT system register on COMPARE match. In this revision, the COUNT register is clocked by the CPU clock, so when the CPU clock stops, so does incrementing of COUNT.  
**Fix/Workaround**  
None.
7. **Memory Protection Unit (MPU) is non functional.**  
**Fix/Workaround**  
Do not use the MPU.
8. **The following alternate GPIO function C are not available in revE**  
MACB-WOL on GPIO9 (PA09), MACB-WOL on GPIO18 (PA18), USB-USB\_ID on GPIO21 (PA21), USB-USB\_VBOF on GPIO22 (PA22), and all function B and C on GPIO70 to GPIO101 (PX00 to PX39).  
**Fix/Workaround**  
Do not use these alternate B and C functions on the listed GPIO pins.
9. **Clock connection table on Rev E**  
  
Here is the table of Rev E

Figure 15-1. Timer/Counter clock connections on RevE

| Source   | Name         | Connection        |
|----------|--------------|-------------------|
| Internal | TIMER_CLOCK1 | 32 KHz Oscillator |
|          | TIMER_CLOCK2 | PBA Clock / 4     |
|          | TIMER_CLOCK3 | PBA Clock / 8     |
|          | TIMER_CLOCK4 | PBA Clock / 16    |
|          | TIMER_CLOCK5 | PBA Clock / 32    |
| External | XC0          |                   |
|          | XC1          |                   |
|          | XC2          |                   |

10. **Local Bus fast GPIO not available in RevE.**  
**Fix/Workaround**  
Do not use on this silicon revision.
11. **Spurious interrupt may corrupt core SR mode to exception**  
If the rules listed in the chapter `Masking interrupt requests in peripheral modules' of the AVR32UC Technical Reference Manual are not followed, a spurious interrupt may occur. An interrupt context will be pushed onto the stack while the core SR mode will indicate an exception. A RETE instruction would then corrupt the stack..  
**Fix/Workaround**  
Follow the rules of the AVR32UC Technical Reference Manual. To increase software robustness, if an exception mode is detected at the beginning of an interrupt handler, change the stack interrupt context to an exception context and issue a RETE instruction.

**12. CPU cannot operate on a divided slow clock (internal RC oscillator)****Fix/Workaround**

Do not run the CPU on a divided slow clock.

**15.3.6 SDRAMC****1. Code execution from external SDRAM does not work**

Code execution from SDRAM does not work.

**Fix/Workaround**

Do not run code from SDRAM..

**2. SDRAM SDCKE rise at the same time as SDCK while exiting self-refresh mode**

SDCKE rise at the same time as SDCK while exiting self-refresh mode.

**Fix/Workaround**

None.

**15.3.7 USART****1. USART Manchester Encoder Not Working**

Manchester encoding/decoding is not working.

**Fix/Workaround**

Do not use manchester encoding.

**2. USART RXBREAK problem when no timeguard**

In asynchronous mode the RXBREAK flag is not correctly handled when the timeguard is 0 and the break character is located just after the stop bit.

**Fix/Workaround**

If the NBSTOP is 1, timeguard should be different from 0.

**3. USART Handshaking: 2 characters sent / CTS rises when TX**

If CTS switches from 0 to 1 during the TX of a character, if the Holding register is not empty, the TXHOLDING is also transmitted.

**Fix/Workaround**

None.

**4. USART PDC and TIMEGUARD not supported in MANCHESTER**

Manchester encoding/decoding is not working.

**Fix/Workaround**

Do not use manchester encoding.

**5. USART SPI mode is non functional on this revision.****Fix/Workaround**

Do not use the USART SPI mode.

**6. DCD is active High instead of Low.**

In modem mode the DCD signal is assumed to be active high by the USART, but should have been active low.

**Fix/Workaround**

Add an external inverter to the DCD line.

### 15.3.8 Power Manager

1. **Voltage regulator input and output is connected to VDDIO and VDDCORE inside the device**

The voltage regulator input and output is connected to VDDIO and VDDCORE respectively inside the device.

**Fix/Workaround**

Do not supply VDDCORE externally, as this supply will work in parallel with the regulator.

2. **Wrong reset causes when BOD is activated**

Setting the BOD enable fuse will cause the Reset Cause Register to list BOD reset as the reset source even though the part was reset by another source.

**Fix/Workaround**

Do not set the BOD enable fuse, but activate the BOD as soon as your program starts.

3. **PLL0/1 Lock control does not work**

Lock Control does not work for PLL0 and PLL1.

**Fix/Workaround**

In PLL0/1 Control register, the bit 7 should be set in order to prevent unexpected behaviour.

4. **Peripheral Bus A maximum frequency is 33MHz instead of 66MHz.**

**Fix/Workaround**

Do not set PBA frequency higher than 33 MHz.

5. **PCx pins go low in stop mode**

In sleep mode stop all PCx pins will be controlled by GPIO module instead of oscillators. This can cause drive contention on the XINx in worst case.

**Fix/Workaround**

Before entering stop mode set all PCx pins to input and GPIO controlled.

6. **On some rare parts, the maximum HSB and CPU speed is 50MHz instead of 66MHz.**

**Fix/Workaround**

Do not set the HSB/CPU speed higher than 50MHz when the firmware generate exceptions.

7. **If the BOD level is higher than VDDCORE, the part is constantly resetted**

If the BOD level is set to a value higher than VDDCORE and enabled by fuses, the part will be in constant reset.

**Fix/Workaround**

Apply an external voltage on VDDCORE that is higher than the BOD level and is lower than VDDCORE max and disable the BOD.

8. **System Timer mask (Bit 16) of the PM CPUMASK register is not available.**

**Fix/Workaround**

Do not use this bit.

### 15.3.9 HMatrix

**1. HMatrix fixed priority arbitration does not work**

Fixed priority arbitration does not work.

**Fix/Workaround**

Use Round-Robin arbitration instead.

### 15.3.10 ADC

**1. ADC possible miss on DRDY when disabling a channel**

The ADC does not work properly when more than one channel is enabled.

**Fix/Workaround**

Do not use the ADC with more than one channel enabled at a time.

**2. ADC OVRE flag sometimes not reset on Status Register read**

The OVRE flag does not clear properly if read simultaneously to an end of conversion.

**Fix/Workaround**

None.

**3. Sleep Mode activation needs additionnal A to D conversion**

If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

**Fix/Workaround**

Activate the sleep mode in the mode register and then perform an AD conversion.

### 15.3.11 ABDAC

**1. Audio Bitstream DAC is not functional.**

**Fix/Workaround**

Do not use the ABDAC on revE.

### 15.3.12 FLASHC

**1. The address of Flash General Purpose Fuse Register Low (FGPFRLO) is 0xFFFE140C on revE instead of 0xFFFE1410.**

**Fix/Workaround**

None.

**2. The command Quick Page Read User Page(QPRUP) is not functional.**

**Fix/Workaround**

None.

**3. PAGEN Semantic Field for Program GP Fuse Byte is WriteData[7:0], ByteAddress[1:0] on revision E instead of WriteData[7:0], ByteAddress[2:0].**

**Fix/Workaround**

None.

**4. On AT32UC3A0512 and AT32UC3A1512, corrupted read in flash after FLASHC WP, EP, EA, WUP, EUP commands may happen**

- After a FLASHC Write Page (WP) or Erase Page (EP) command applied to a page in a given half of the flash (first or last 256 kB of flash), reading (data read or code fetch) the other half of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.
- After a FLASHC Erase All (EA) command, reading (data read or code fetch) the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.
- After a FLASHC Write User Page (WUP) or Erase User Page (EUP) command, reading (data read or code fetch) the second half (last 256 kB) of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

**Fix/Workaround**

Flashc WP, EP, EA, WUP, EUP commands: these commands must be issued from RAM or through the EBI. After these commands, read twice one flash page initialized to 00h in each half part of the flash.

**15.3.13 RTC**

1. **Writes to control (CTRL), top (TOP) and value (VAL) in the RTC are discarded if the RTC peripheral bus clock (PBA) is divided by a factor of four or more relative to the HSB clock.**

**Fix/Workaround**

Do not write to the RTC registers using the peripheral bus clock (PBA) divided by a factor of four or more relative to the HSB clock.

2. **The RTC CLKEN bit (bit number 16) of CTRL register is not available.**

**Fix/Workaround**

Do not use the CLKEN bit of the RTC on Rev E.

**15.3.14 OCD**

1. **Stalled memory access instruction writeback fails if followed by a HW breakpoint.**

Consider the following assembly code sequence:

A

B

If a hardware breakpoint is placed on instruction B, and instruction A is a memory access instruction, register file updates from instruction A can be discarded.

**Fix/Workaround**

Do not place hardware breakpoints, use software breakpoints instead.

Alternatively, place a hardware breakpoint on the instruction before the memory access instruction and then single step over the memory access instruction.

## 16. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

### 16.1 Rev. E – 04/08

1. Open Drain Mode removed from "General-Purpose Input/Output Controller (GPIO)" on page 151.

### 16.2 Rev. D – 04/08

1. Updated "Signal Description List" on page 8. Removed RXDN and TXDN from USART section.
2. Updated "Errata" on page 64. Rev G replaced by rev H.

### 16.3 Rev. C – 10/07

1. Updated "Signal Description List" on page 8. Removed RXDN and TXDN from USART section.
2. Updated "Errata" on page 64. Rev G replaced by rev H.

### 16.4 Rev. B – 10/07

1. Updated "Features" on page 1.
2. Update "Blockdiagram" on page 4 with local bus.
3. Updated "Peripherals" on page 34 with local bus.
4. Add SPI feature in "Universal Synchronous/Asynchronous Receiver/Transmitter (USART)" on page 315.
5. Updated "USB On-The-Go Interface (USBB)" on page 517.
6. Updated "JTAG and Boundary Scan" on page 750 with programming procedure .
7. Add description for silicon Rev G.

### 16.5 Rev. A – 03/07

1. Initial revision.

KTTIC

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