



IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

HIGH AND LOW SIDE DRIVER

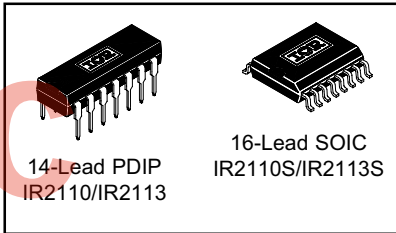
Features

- Floating channel designed for bootstrap operation
Fully operational to +500V or +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
Separate logic supply range from 3.3V to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET} (IR2110)	500V max.
(IR2113)	600V max.
$I_{O+/-}$	2A / 2A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	120 & 94 ns
Delay Matching (IR2110)	10 ns max.
(IR2113)	20ns max.

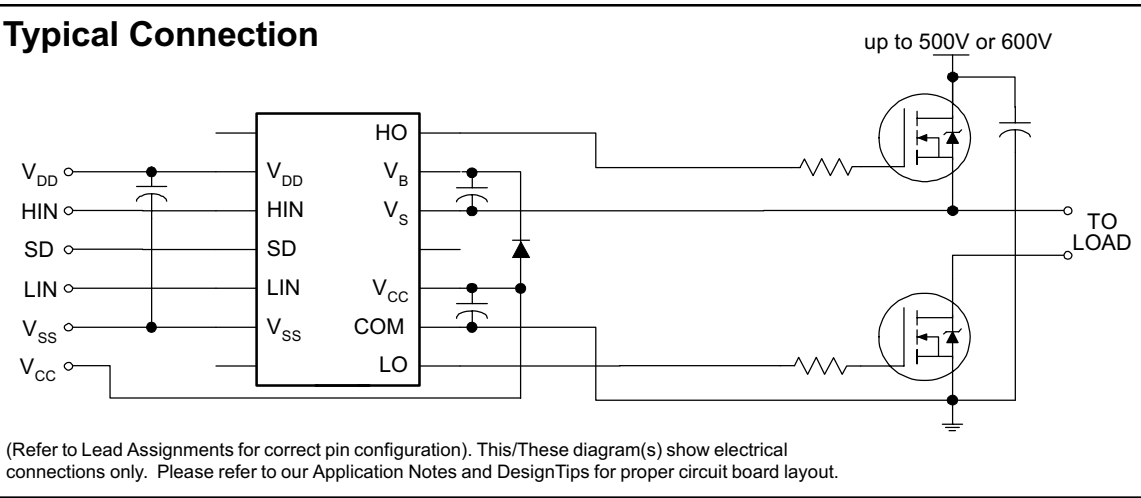
Packages



Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply voltage (IR2110)	-0.3	525	V
	(IR2113)	-0.3	625	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3	
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side fixed supply voltage	-0.3	25	
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3	
V _{DD}	Logic supply voltage	-0.3	V _{SS} + 25	
V _{SS}	Logic supply offset voltage	V _{CC} - 25	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN, LIN & SD)	V _{SS} - 0.3	V _{DD} + 0.3	
dV _S /dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns
P _D	Package power dissipation @ T _A ≤ +25°C (14 lead DIP)	—	1.6	W
	(16 lead SOIC)	—	1.25	
R _{THJA}	Thermal resistance, junction to ambient (14 lead DIP)	—	75	°C/W
	(16 lead SOIC)	—	100	
T _J	Junction temperature	—	150	°C
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage (IR2110)	Note 1	500	
	(IR2113)	Note 1	600	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side fixed supply voltage	10	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{DD}	Logic supply voltage	V _{SS} + 3	V _{SS} + 20	
V _{SS}	Logic supply offset voltage	-5 (Note 2)	5	
V _{IN}	Logic input voltage (HIN, LIN & SD)	V _{SS}	V _{DD}	°C
T _A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Note 2: When V_{DD} < 5V, the minimum V_{SS} offset is limited to -V_{DD}.



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Dynamic Electrical Characteristics

VBIAS (VCC, VBS, VDD) = 15V, CL = 1000 pF, TA = 25°C and VSS = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
ton	Turn-on propagation delay	7	—	120	150	ns	VS = 0V
toff	Turn-off propagation delay	8	—	94	125		VS = 500V/600V
tSD	Shutdown propagation delay	9	—	110	140		VS = 500V/600V
tr	Turn-on rise time	10	—	25	35		
tf	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off	(IR2110) (IR2113)	—	—	—		10 20

Static Electrical Characteristics

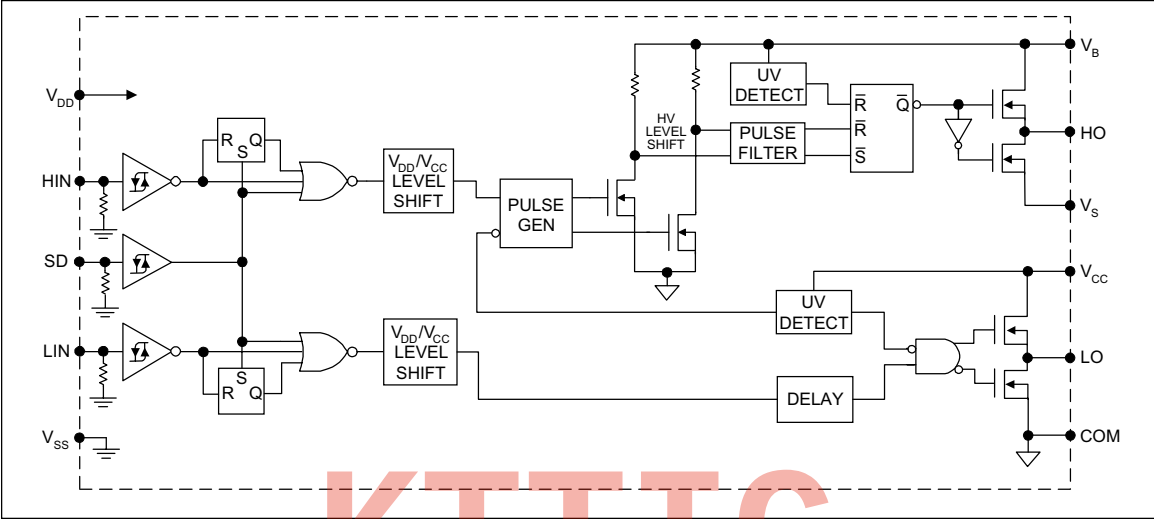
VBIAS (VCC, VBS, VDD) = 15V, TA = 25°C and VSS = COM unless otherwise specified. The VIN, VTH and IIN parameters are referenced to VSS and are applicable to all three logic input leads: HIN, LIN and SD. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
VIH	Logic “1” input voltage	12	9.5	—	—	V	
VIL	Logic “0” input voltage	13	—	—	6.0		
VOH	High level output voltage, VBIAS - VO	14	—	—	1.2		IO = 0A
VOL	Low level output voltage, VO	15	—	—	0.1		IO = 0A
ILK	Offset supply leakage current	16	—	—	50	µA	VB=VS = 500V/600V
IQBS	Quiescent VBS supply current	17	—	125	230		VIN = 0V or VDD
IQCC	Quiescent VCC supply current	18	—	180	340		VIN = 0V or VDD
IQDD	Quiescent VDD supply current	19	—	15	30		VIN = 0V or VDD
IIN+	Logic “1” input bias current	20	—	20	40		VIN = VDD
IIN-	Logic “0” input bias current	21	—	—	1.0		VIN = 0V
VBSUV+	VBS supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
VBSUV-	VBS supply undervoltage negative going threshold	23	7.0	8.2	9.4		
VCCUV+	VCC supply undervoltage positive going threshold	24	7.4	8.5	9.6		
VCCUV-	VCC supply undervoltage negative going threshold	25	7.0	8.2	9.4		
IO+	Output high short circuit pulsed current	26	2.0	2.5	—	A	VO = 0V, VIN = VDD PW ≤ 10 µs
IO-	Output low short circuit pulsed current	27	2.0	2.5	—		VO = 15V, VIN = 0V PW ≤ 10 µs

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Functional Block Diagram



Lead Definitions

Symbol	Description
VDD	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

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Lead Assignments

14 Lead PDIP IR2110/IR2113	16 Lead SOIC (Wide Body) IR2110S/IR2113S
14 Lead PDIP w/o lead 4 IR2110-1/IR2113-1	14 Lead PDIP w/o leads 4 & 5 IR2110-2/IR2113-2
Part Number	

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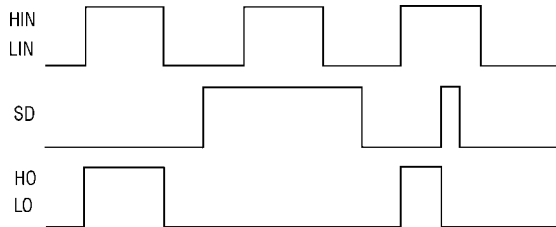


Figure 1. Input/Output Timing Diagram

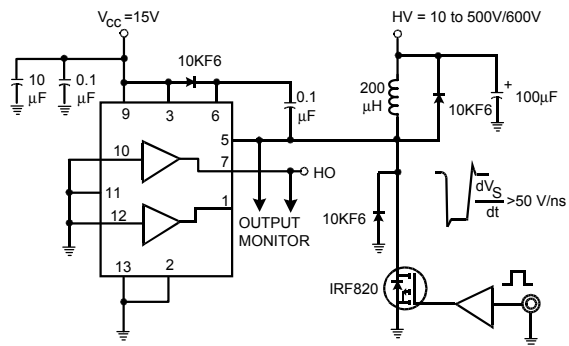


Figure 2. Floating Supply Voltage Transient Test Circuit

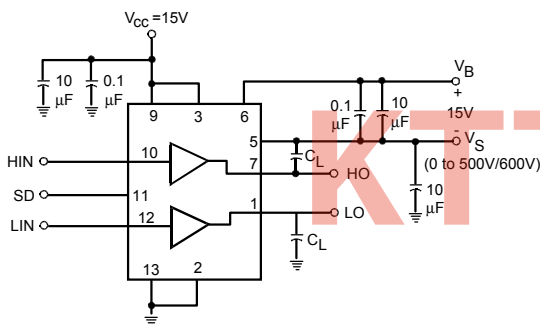


Figure 3. Switching Time Test Circuit

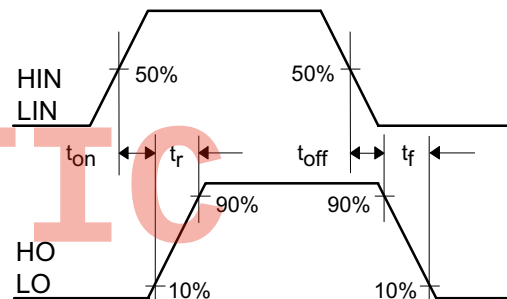


Figure 4. Switching Time Waveform Definition

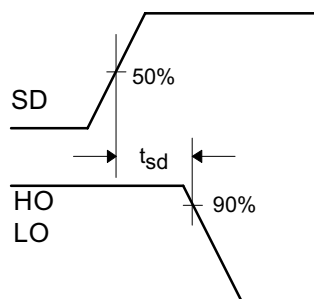


Figure 5. Shutdown Waveform Definitions

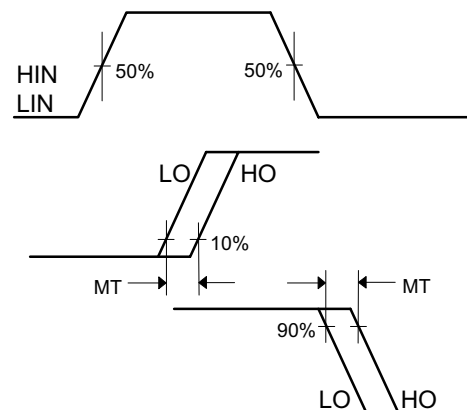


Figure 6. Delay Matching Waveform Definitions

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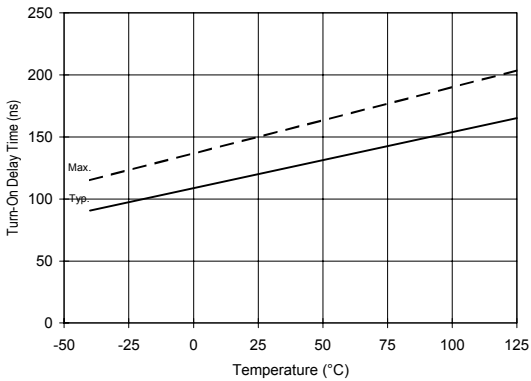


Figure 7A. Turn-On Time vs. Temperature

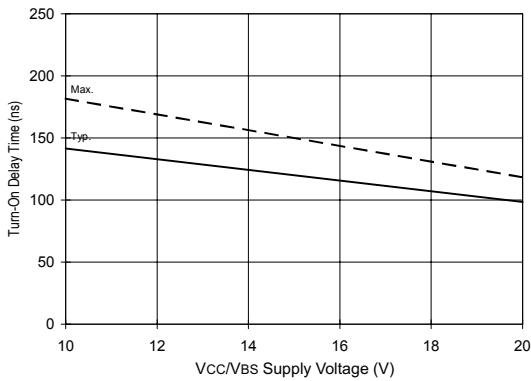


Figure 7B. Turn-On Time vs. Vcc/Vbs Supply Voltage

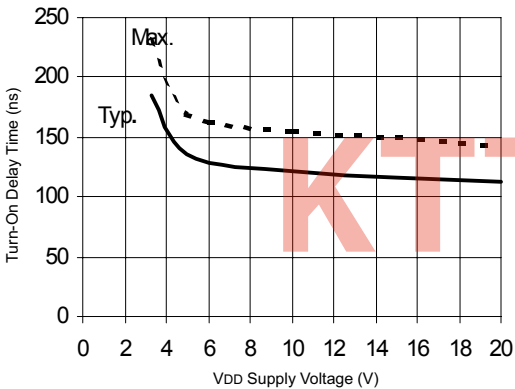


Figure 7C. Turn-On Time vs. VDD Supply Voltage

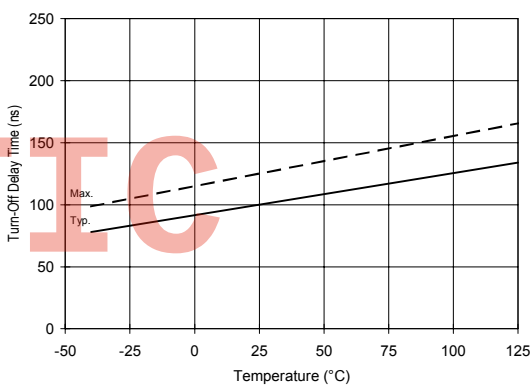


Figure 8A. Turn-Off Time vs. Temperature

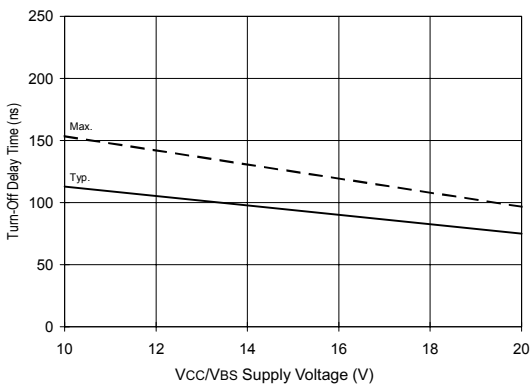


Figure 8B. Turn-Off Time vs. Vcc/Vbs Supply Voltage

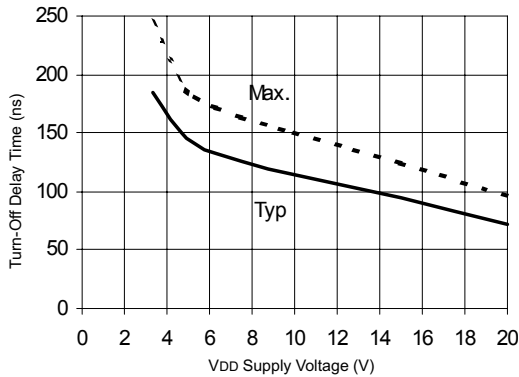


Figure 8C. Turn-Off Time vs. VDD Supply Voltage

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

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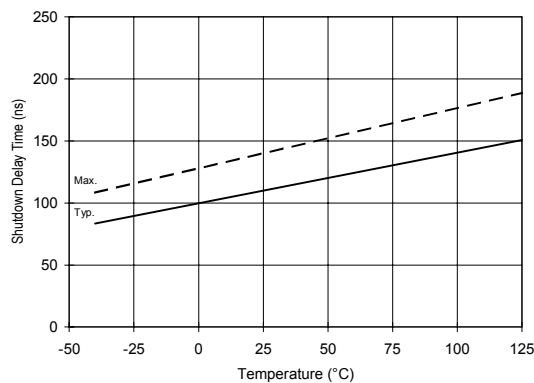


Figure 9A. Shutdown Time vs. Temperature

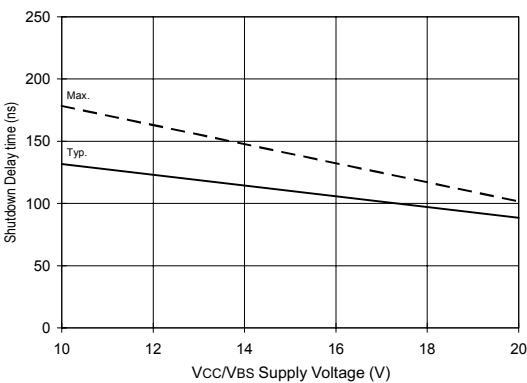


Figure 9B. Shutdown Time vs. Vcc/Vbs Supply Voltage

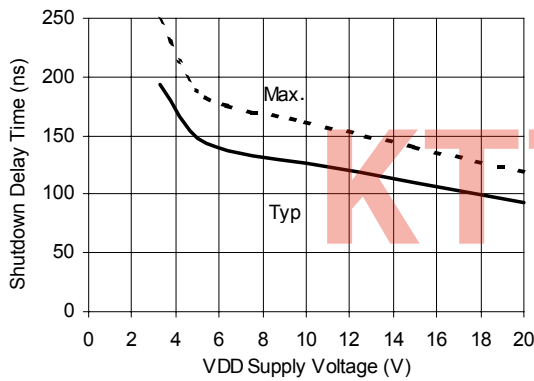


Figure 9C. Shutdown Time vs. VDD Supply Voltage

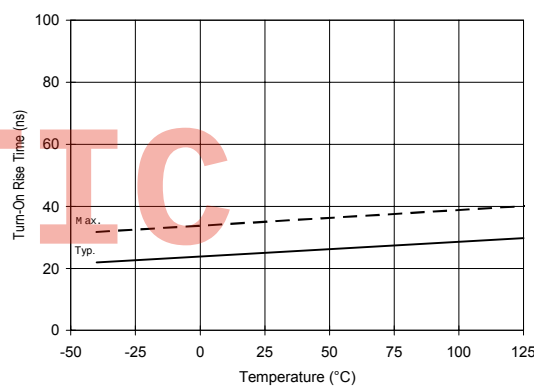


Figure 10A. Turn-On Rise Time vs. Temperature

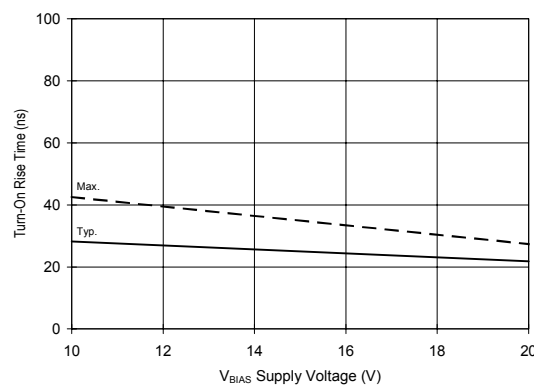


Figure 10B. Turn-On Rise Time vs. Voltage

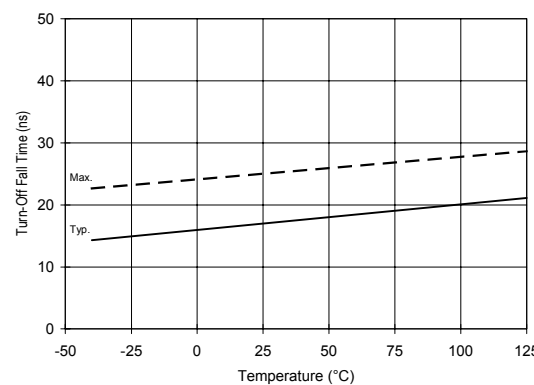


Figure 11A. Turn-Off Fall Time vs. Temperature

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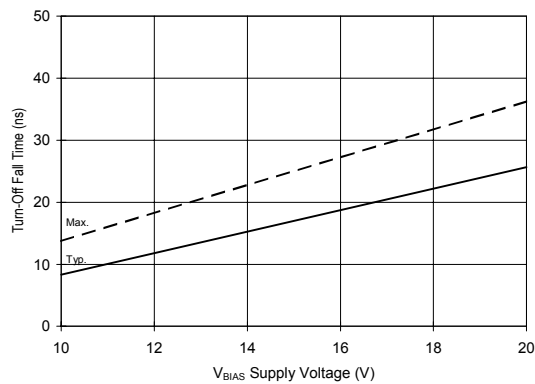


Figure 11B. Turn-Off Fall Time vs. Voltage

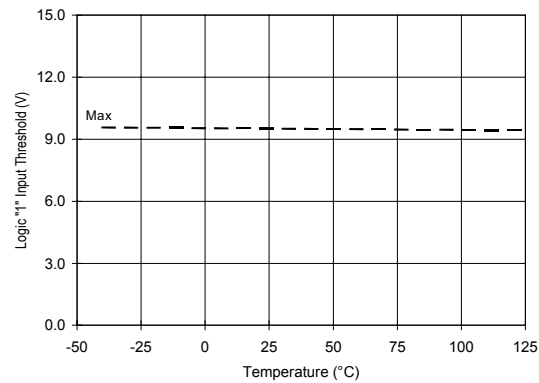


Figure 12A. Logic "1" Input Threshold vs. Temperature

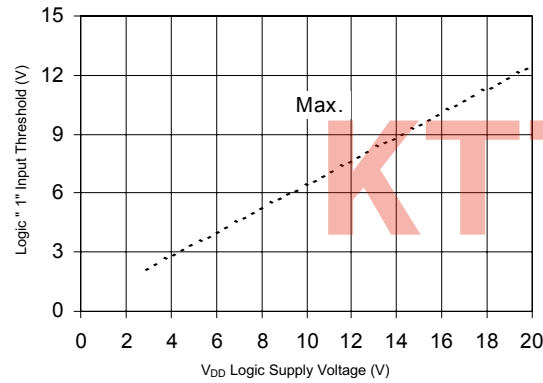


Figure 12B. Logic "1" Input Threshold vs. Voltage

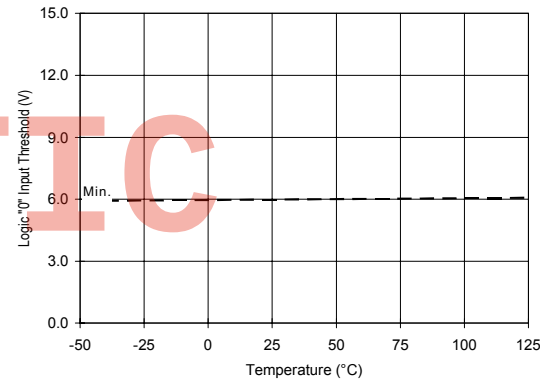


Figure 13A. Logic "0" Input Threshold vs. Temperature

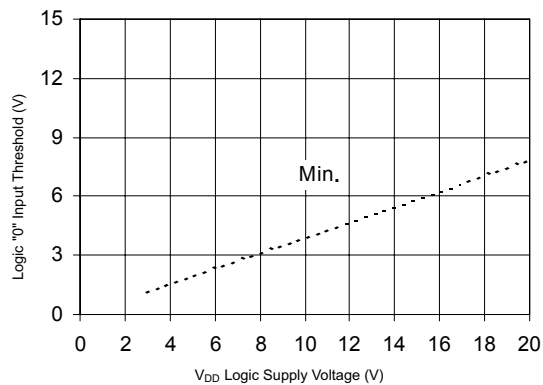


Figure 13B. Logic "0" Input Threshold vs. Voltage

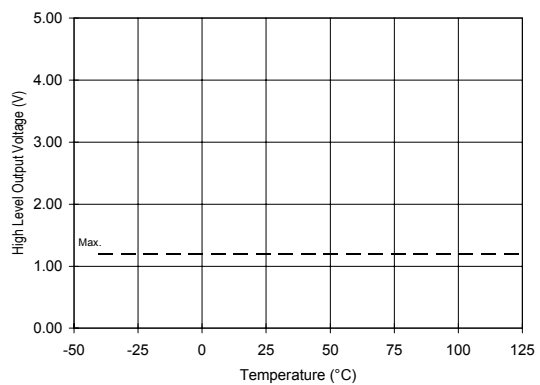


Figure 14A. High Level Output vs. Temperature

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

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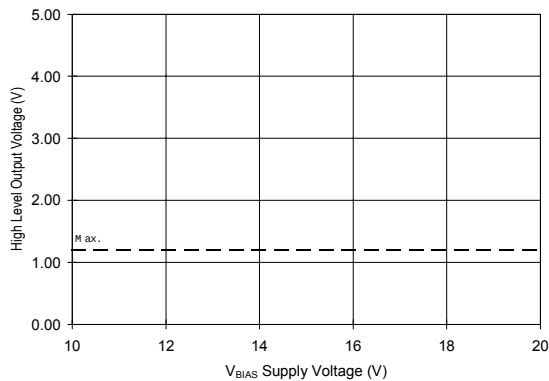


Figure 14B. High Level Output vs. Voltage

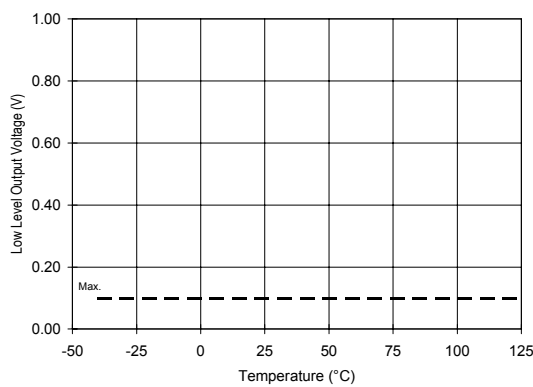


Figure 15A. Low Level Output vs. Temperature

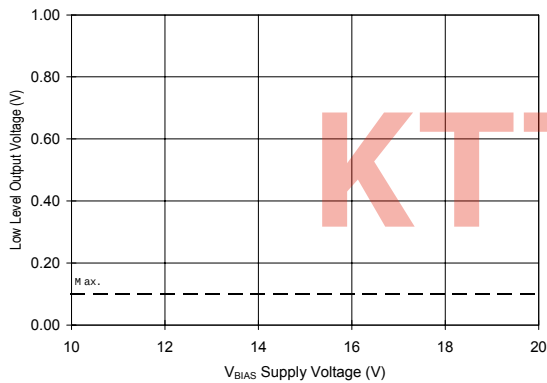


Figure 15B. Low Level Output vs. Voltage

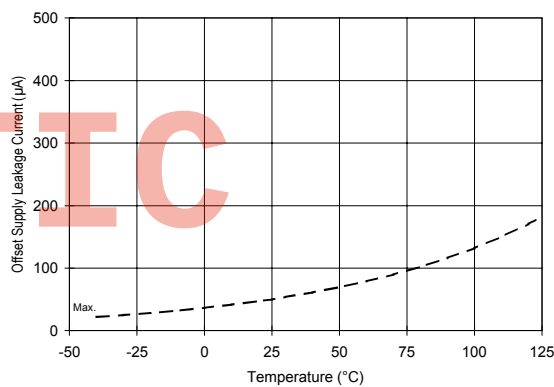


Figure 16A. Offset Supply Current vs. Temperature

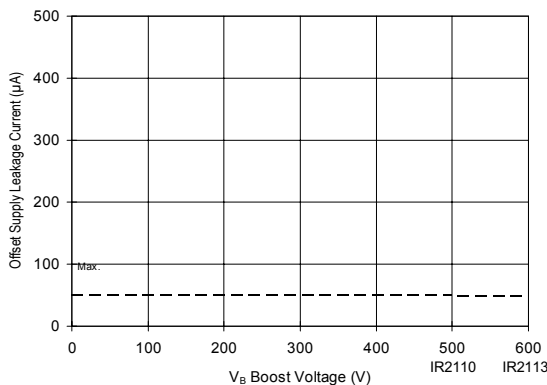


Figure 16B. Offset Supply Current vs. Voltage

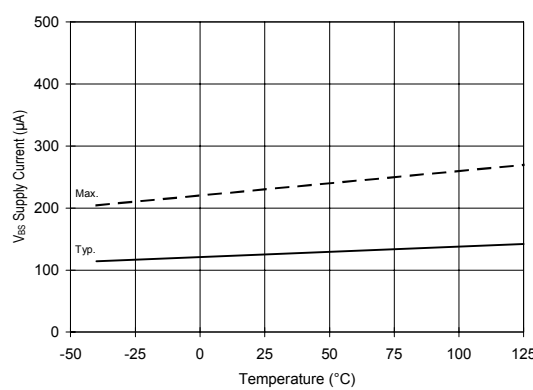


Figure 17A. V_{BS} Supply Current vs. Temperature

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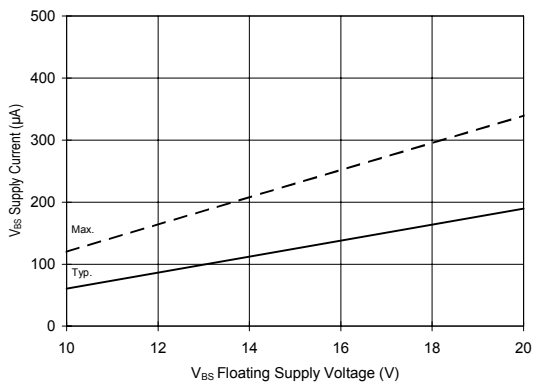


Figure 17B. V_{BS} Supply Current vs. Voltage

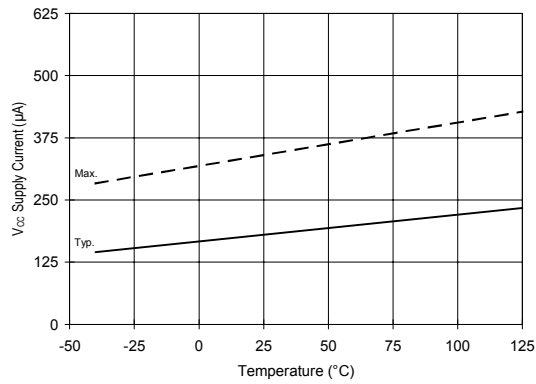


Figure 18A. V_{CC} Supply Current vs. Temperature

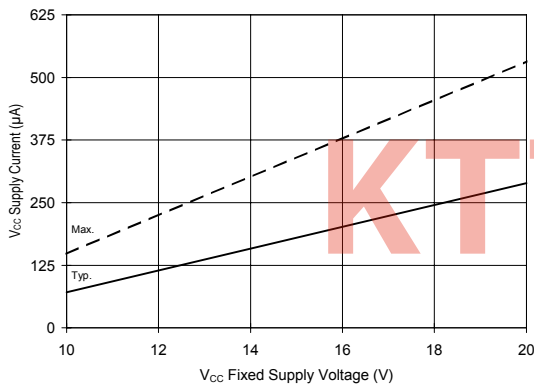


Figure 18B. V_{CC} Supply Current vs. Voltage

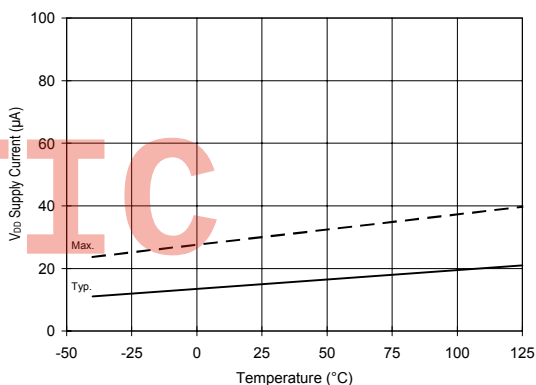


Figure 19A. V_{DD} Supply Current vs. Temperature

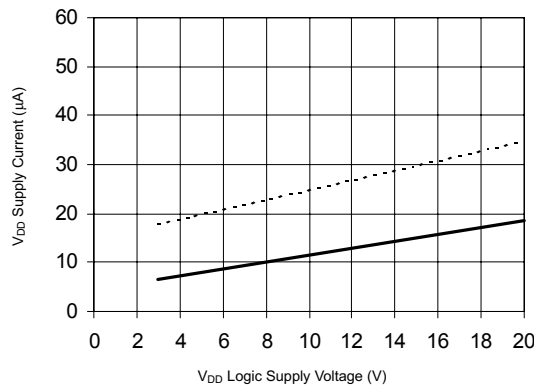


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

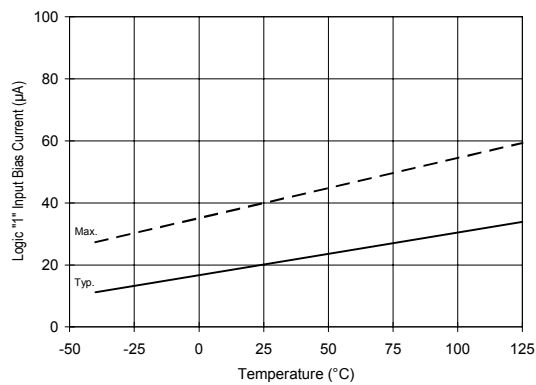


Figure 20A. Logic "1" Input Current vs. Temperature

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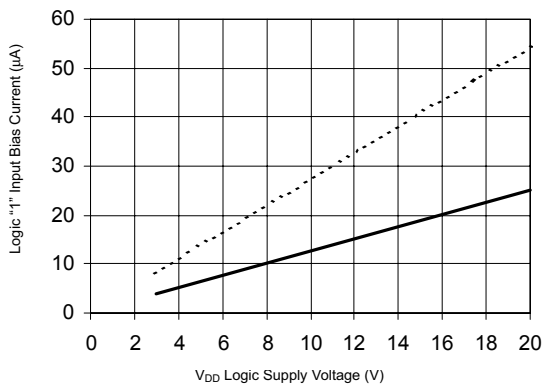


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

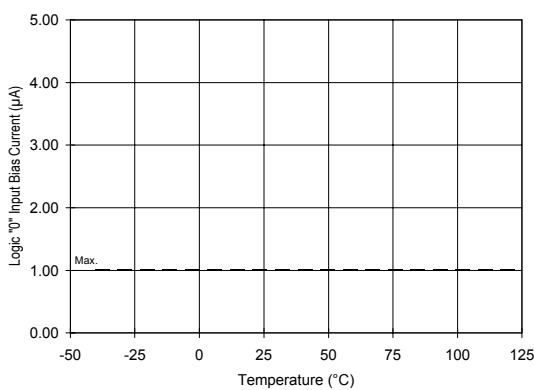


Figure 21A. Logic "0" Input Current vs. Temperature

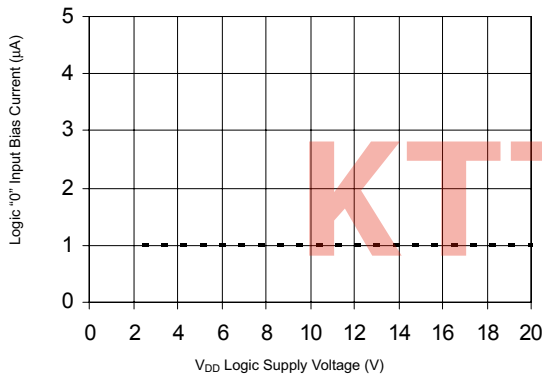


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

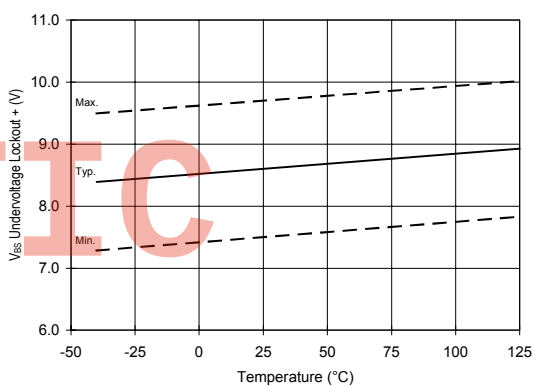


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

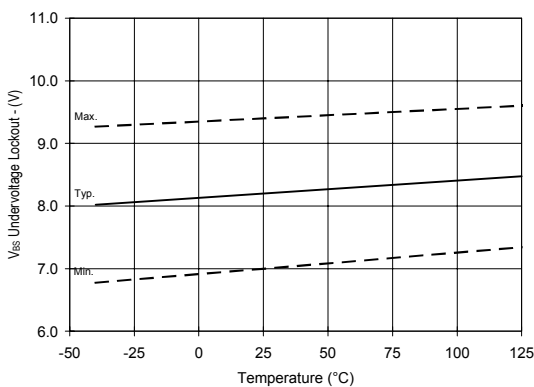


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

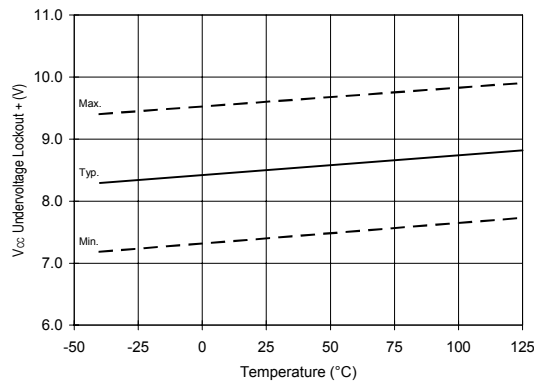


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

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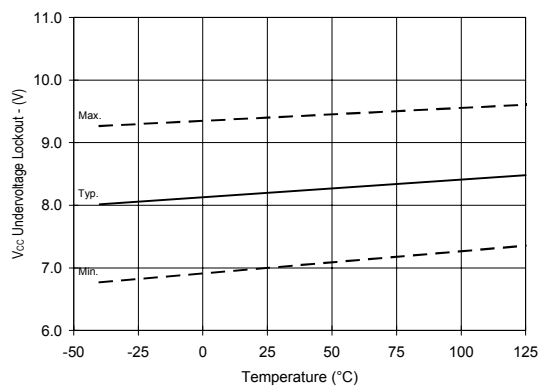


Figure 25. Vcc Undervoltage (-) vs. Temperature

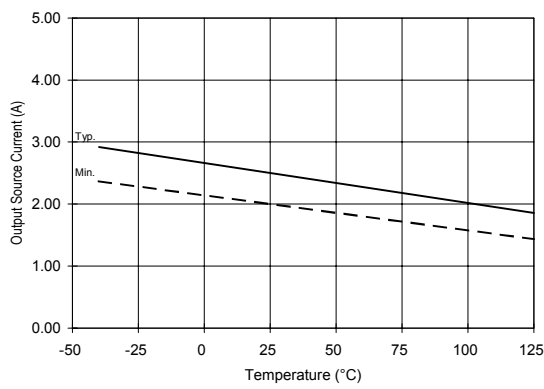


Figure 26A. Output Source Current vs. Temperature

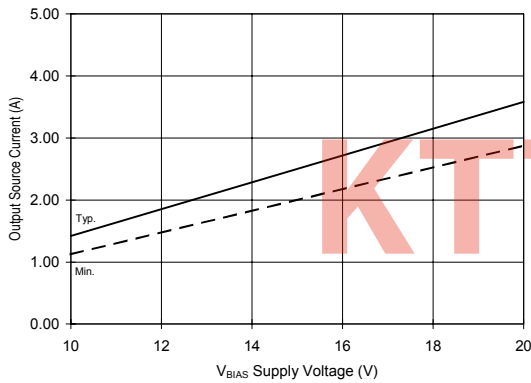


Figure 26B. Output Source Current vs. Voltage

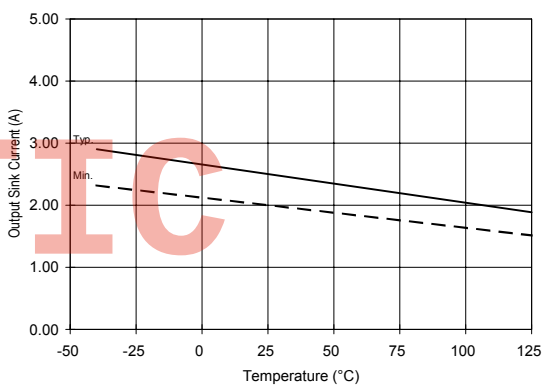


Figure 27A. Output Sink Current vs. Temperature

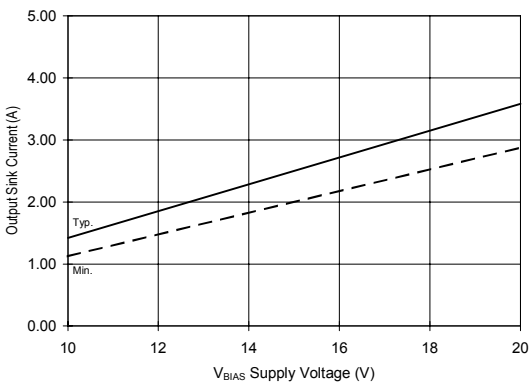


Figure 27B. Output Sink Current vs. Voltage

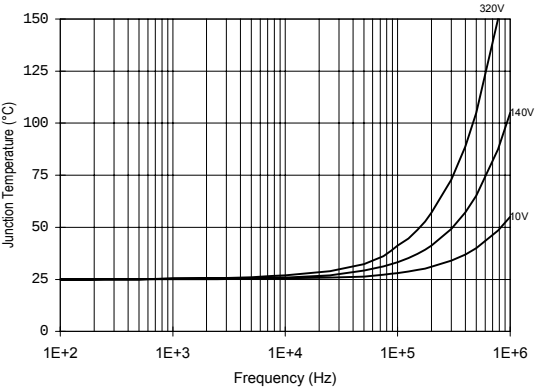


Figure 28. IR2110/IR2113 T_J vs. Frequency
(IRFBC20) $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

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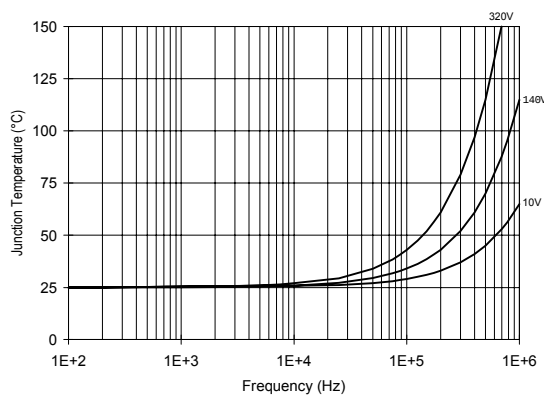


Figure 29. IR2110/IT2113 T_J vs. Frequency (IRFBC30) $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

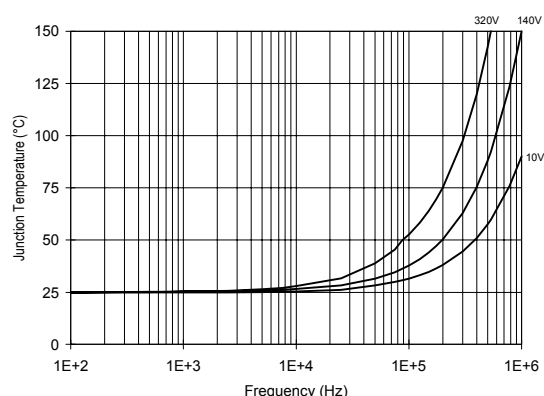


Figure 30. IR2110/IR2113 T_J vs. Frequency (IRFBC40) $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

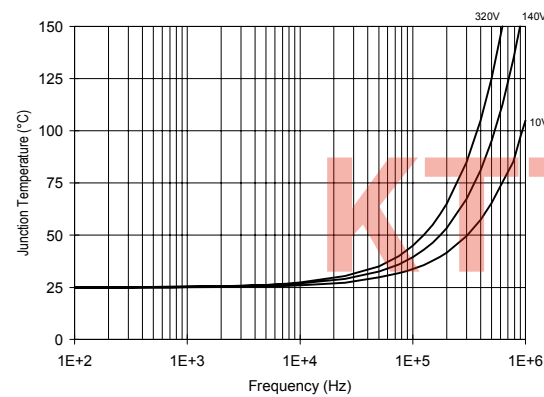


Figure 31. IR2110/IR2113 T_J vs. Frequency (IRFPE50) $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

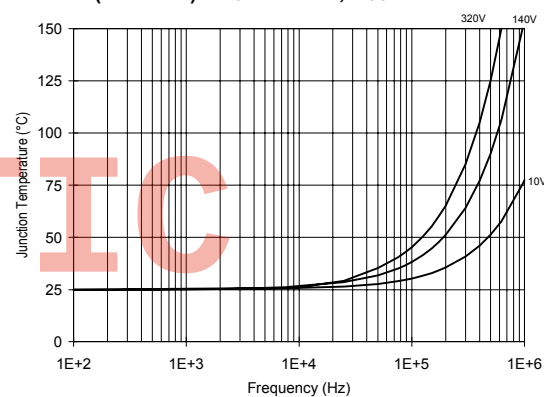


Figure 32. IR2110S/IR2113S T_J vs. Frequency (IRFBC20) $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

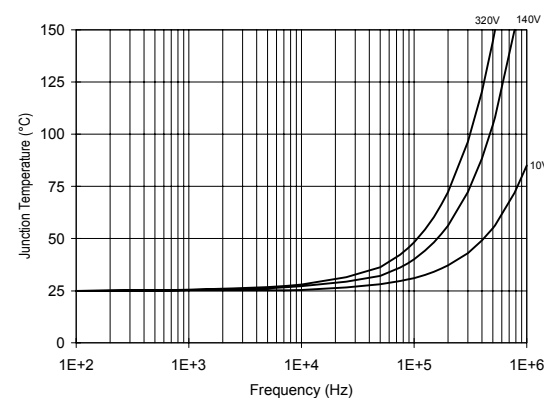


Figure 33. IR2110S/IR2113S T_J vs. Frequency (IRFBC30) $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

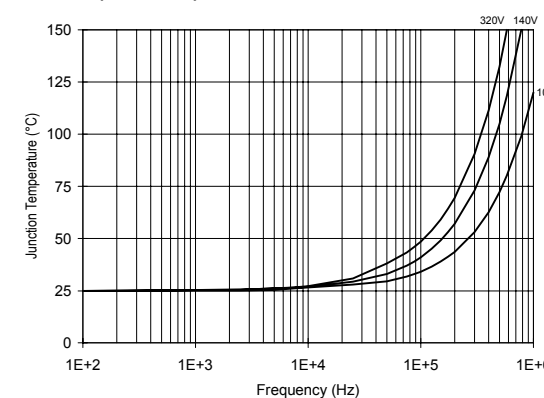


Figure 34. IR2110S/IR2113S T_J vs. Frequency (IRFBC40) $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

International
IR Rectifier

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

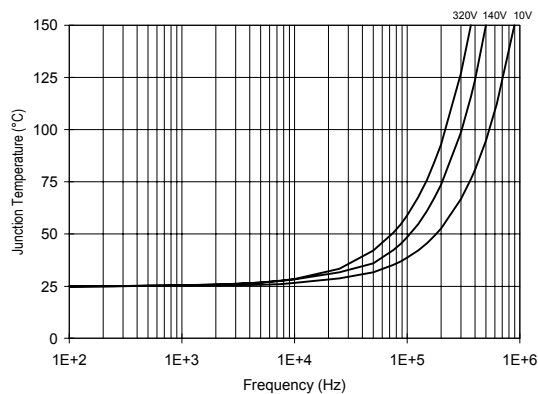


Figure 35. IR2110S/IR2113S T_J vs. Frequency (IRFPE50) $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

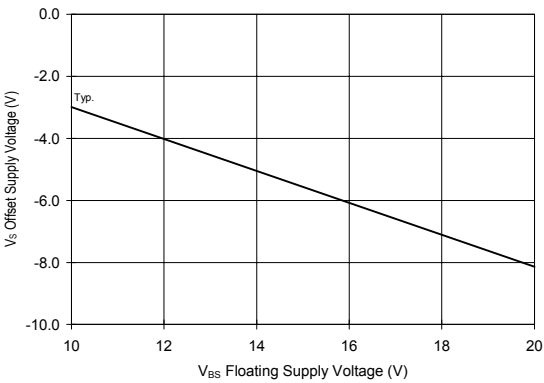


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

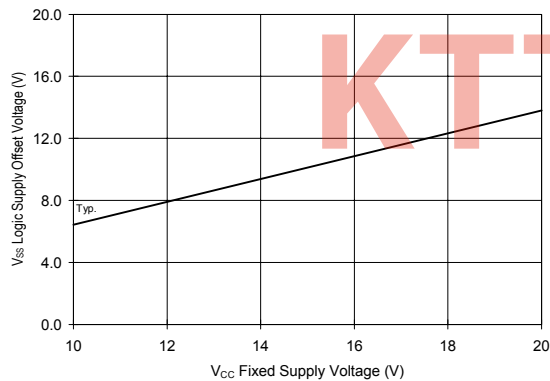
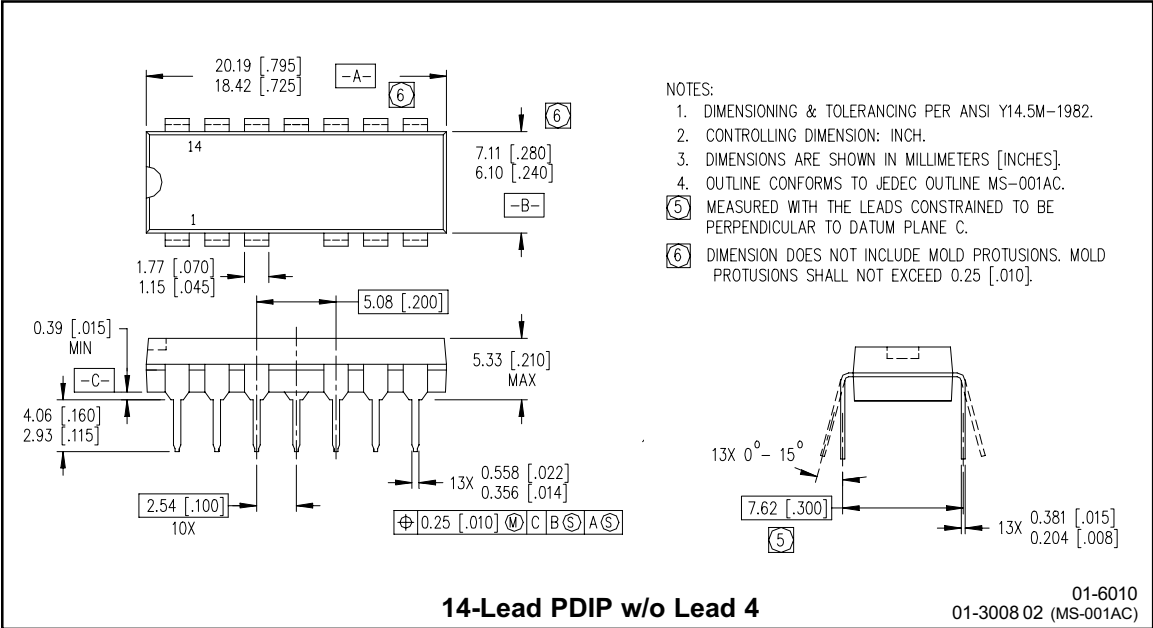
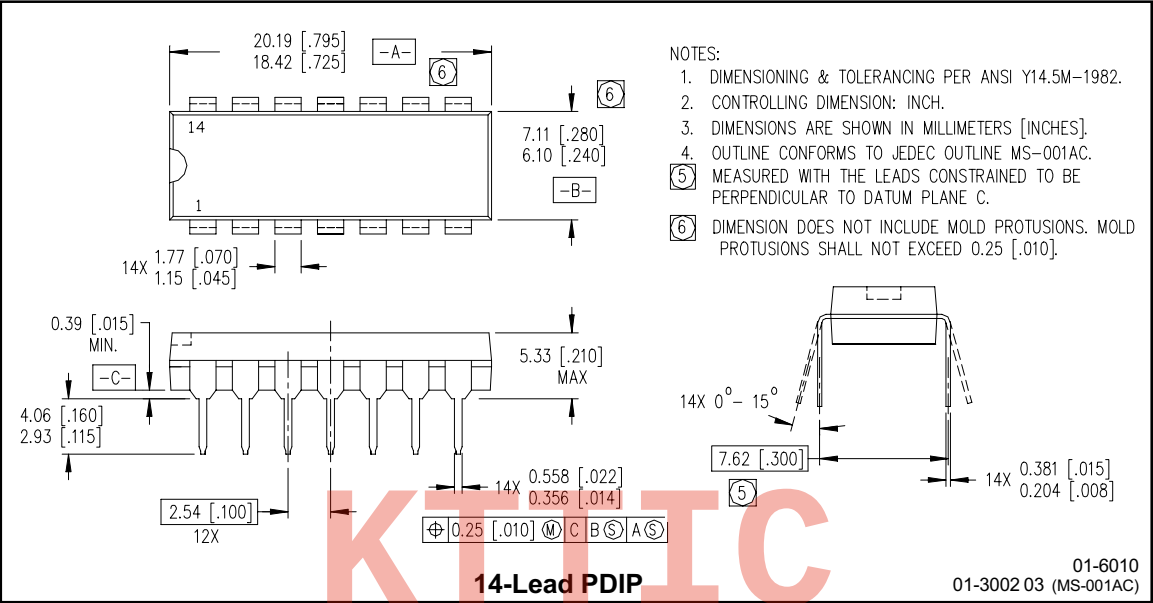


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

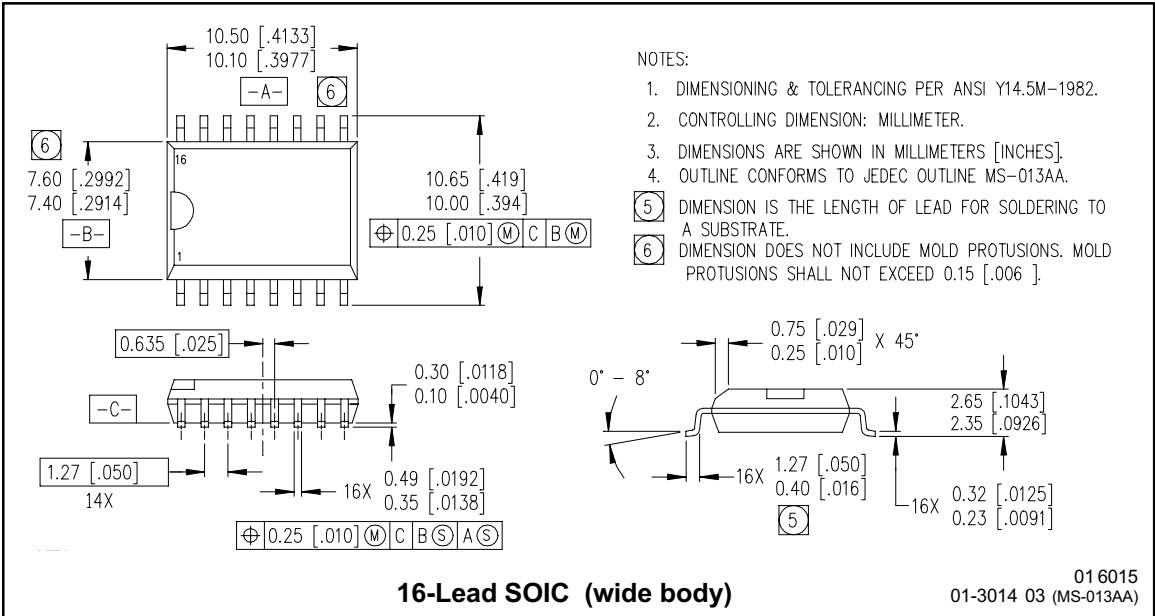
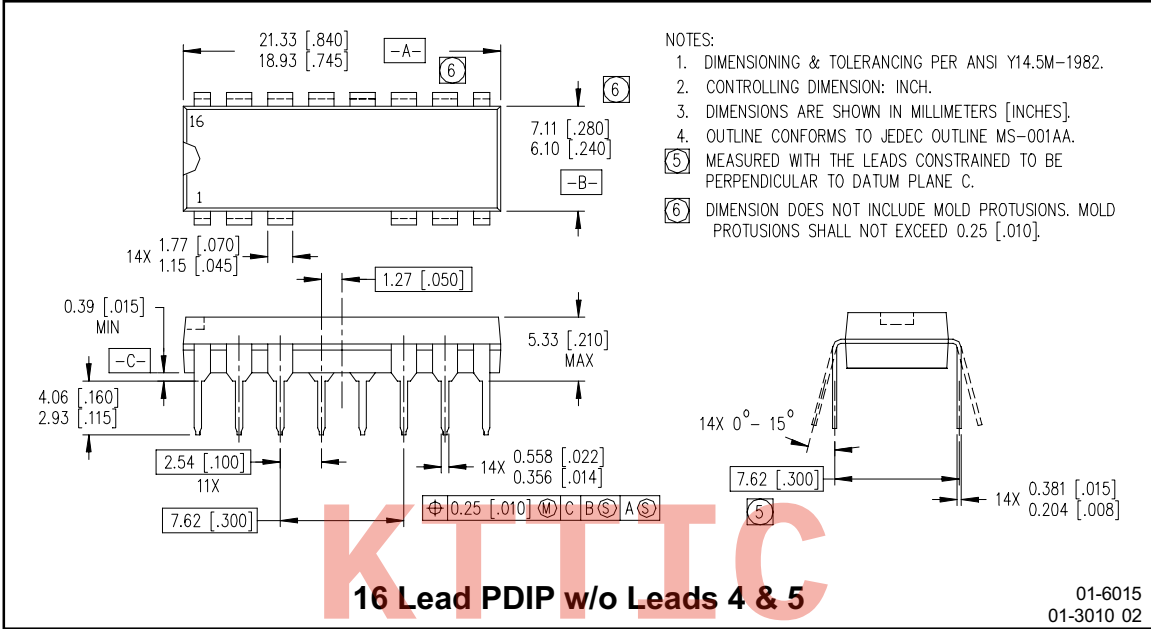
International
IR Rectifier

Case Outlines



International
IR Rectifier

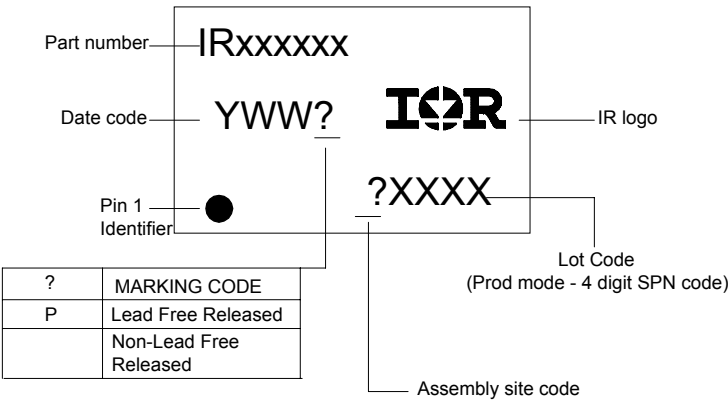
IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF



IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

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LEADFREE PART MARKING INFORMATION



KTTIC
ORDER INFORMATION
Part only available Lead Free

- 14-Lead PDIP IR2110 order IR2110PbF
- 14-Lead PDIP IR2110-1 order IR2110-1PbF
- 14-Lead PDIP IR2110-2 order IR2110-2PbF
- 14-Lead PDIP IR2113 order IR2113PbF
- 14-Lead PDIP IR2113-1 order IR2113-1PbF
- 14-Lead PDIP IR2113-2 order IR2113-2PbF
- 16-Lead SOIC IR2110S order IR2110SPbF
- 16-Lead SOIC IR2113S order IR2113SPbF

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This product has been qualified per industrial level
Data and specifications subject to change without notice 3/23/2005