1   Key Message

The F2803x and F2802x Piccolo™ family of microcontrollers provide the power of the C28x™ core coupled with highly integrated control peripherals in low pincount devices. This family is code compatible with previous C28-based code, as well as providing the highest level of analog integration to date for the C28x family.

An internal voltage regulator allows for single rail operation. Enhancements have been made to the HRPWM module to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3 V fixed full scale range as well as supporting ratiometric VREFHI/VREFLO references, and the interface has been reworked with low overhead/latency in mind.

The F2803x adds a hardware control law accelerator (CLA) with access to memory and several peripherals. Local interconnect network (LIN) and controller area network (CAN) serial protocol controllers are also added to the F2803x.

1.1   Key Features

- **High-Efficiency 32-Bit CPU (TMS320C28x)**
  - **60 MHz (16.67-ns Cycle Time)**
  - **40 MHz (25-ns Cycle Time)**
  - **16 x 16 and 32 x 32 MAC Operations**
  - **16 x 16 Dual MAC**
  - **Harvard Bus Architecture**
  - **Atomic Operations**
  - **Fast Interrupt Response and Processing**
  - **Unified Memory Programming Model**
  - **Code-Efficient (in C/C++ and Assembly)**
- **Low Device & System Cost:**
  - **Single 3.3-V Supply**
  - **No Power Sequencing Requirement**
  - **Integrated Power On Reset & Brown Out Reset**
  - **Small Packaging, as low as 38-pin available**
  - **Low Power**
  - **No Analog Support Pins**
- **Clocking:**
  - **2 Internal Zero Pin Oscillators**
  - **On-Chip Oscillator**
  - **Dynamic PLL Ratio Changes Supported**
  - **Watchdog Timer Module**
  - **Missing Clock Detection Circuitry**
- **Up to 44/22 (2803x/2802x) Individually Programmable, Multiplexed GPIO Pins With Input Filtering**

- **Peripheral Interrupt Expansion (PIE) Block That Supports All Peripheral Interrupts**
- **Three 32-Bit CPU Timers**
- **On-Chip Memory**
  - **Flash, SARAM, OTP, Boot ROM Available**
- **128-Bit Security Key/Lock**
  - **Protects Secure Memory Blocks**
  - **Prevents Firmware Reverse Engineering**
- **Advanced Emulation Features**
  - **Analysis and Breakpoint Functions**
  - **Real-Time Debug via Hardware**
- **Enhanced Control Peripherals**
  - **Enhanced Pulse Width Modulator (ePWM)**
  - **High-resolution PWM (HRPWM)**
  - **Enhanced Capture (eCAP)**
  - **Enhanced Quadrature Encoder Pulse (eQEP)**
  - **Analog-to-Digital Converter (ADC)**
  - **Comparator**
- **2802x Packages**
  - **38-Pin DA Thin Shrink Small Outline Package (TSSOP)**
  - **48-Pin PT Low Profile Quad Flatpack (LQFP)**
- **2803x Packages**
  - **64-Pin PAG Thin Quad Flatpack (TQFP)**
  - **80-Pin PN Low Profile Quad Flatpack (LQFP)**

PRODUCT PREVIEW

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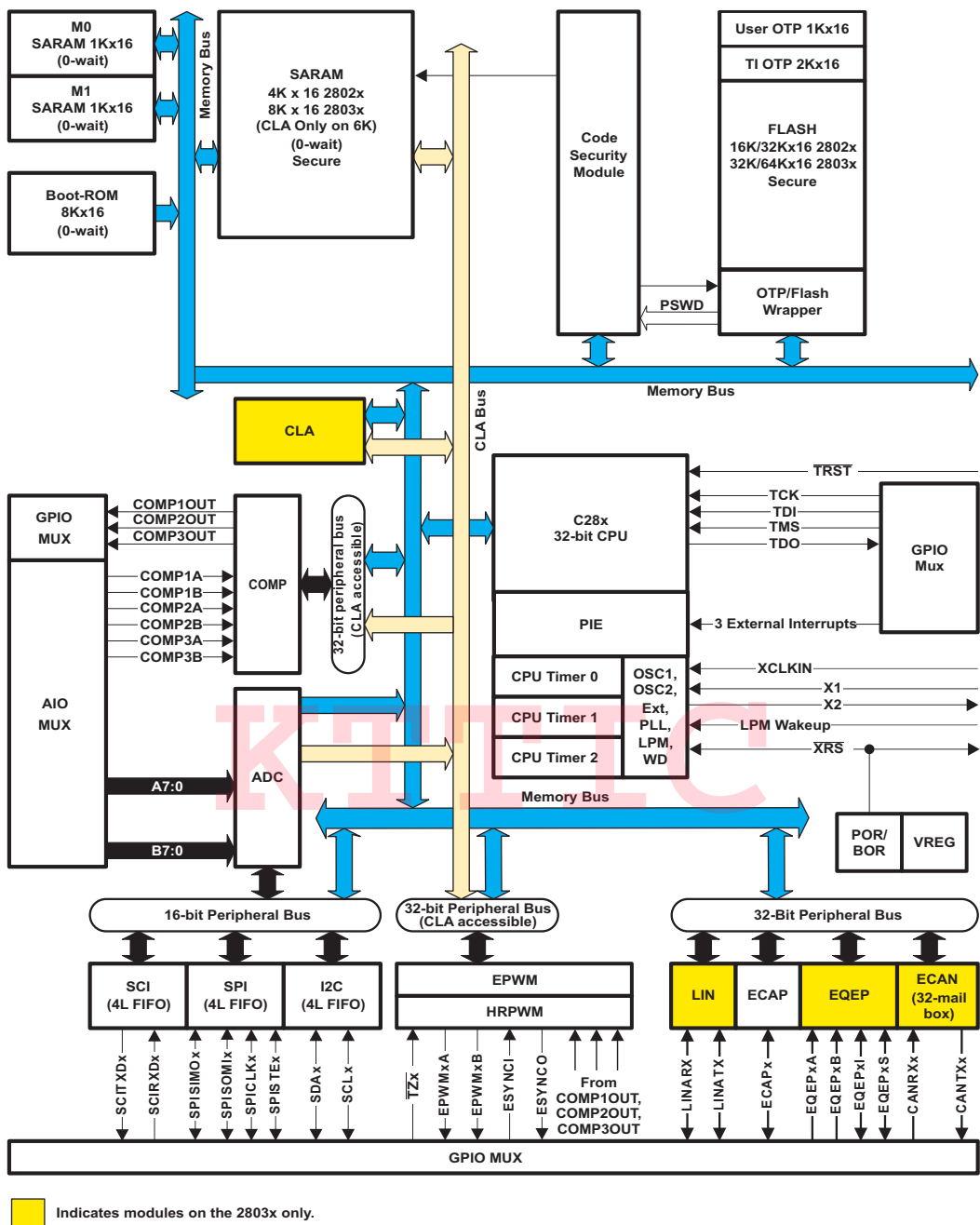
Piccolo, C28x, Code Composer Studio are trademarks of Texas Instruments.

1.2 Functional Block Diagram

PRODUCT PREVIEW

Figure 1-1. Functional Block Diagram

Indicates modules on the 2803x only.

A.   Not all peripheral pins are available at the same time due to multiplexing.

1.2.1 Peripheral Summary

Table 1-1. Peripheral Descriptions

Peripherals	F2802x	F2803x	Type	Description
Control Peripherals				
ePWM	4	7	1	Enchanced pulse width modulation control with independent 16-bit timers per ePWM module
PWM Outputs	Up to 9	Up to 15	-	Pulse width modulation outputs
HRPWM	4	5	1	High Resolution PWM, 150-ps resolution on both edges for duty and frequency control
eCAP	1	1	0	Enhanced Capture Input with independent 32-bit timer
eQEP	-	1	0	Quadrature Encoder Pulse Module with independent 32-bit timer
Communications Peripherals				
SPI	1	2	1	Serial Peripheral Interface with 4-level FIFO
SCI	1	1	0	Serial Communications Interface (UART) with 4-level FIFO
I2C	1	1	0	Inter-Integrated Circuit with 4-level FIFO
LIN	-	1	0	LIN 2.0 controller
CAN	-	1	0	CAN 2.0B controller
Analog Periperals				
ADC	1	1	3	12-bit ADC dual sample and hold, up to 4.6 MSPS sustained conversion rate
ADC Channels	Up to 13	Up to 16	-	ADC input channels
Analog IO Channels	6	6	-	Analog channels that can be used as general purpose I/Os
Comparator	Up to 2	3	0	Analog comparator, with dedicated 10-bit reference
HW Accelerators				
CLA	-	1	0	Independent 32-bit floating point control law accelerator

PRODUCT PREVIEW

2 Key Electrical Characteristics

2.1 Absolute Maximum Ratings[(1)(2)]

Unless otherwise noted, the list of absolute maximum ratings are specified over operating temperature ranges.

Supply voltage range, V_{DDIO}	with respect to V_{SS}	− 0.3 V to 4.0 V
Supply voltage range, V_{DD}	with respect to V_{SS}	− 0.3 V to 2.4 V
Analog voltage range, V_{DDA}	with respect to V_{SSA}	− 0.3 V to 4.0 V
Input voltage range, V_{IN} (3.3 V)		− 0.3 V to 4.0 V
Input voltage range, V_{IN} (1.8 V)		− 0.3 V to 2.4 V
Output voltage range, V_O		− 0.3 V to 4.0 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO}) [(3)]		± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO})		± 20 mA
Operating ambient temperature ranges	T_A: A version	− 40°C to 85°C
	T_A: S version	− 40°C to 125°C
	T_A: Q version	− 40°C to 125°C
Junction temperature range, T_j		− 40°C to 150°C
Storage temperature range, T_{stg}		− 65°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 2.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ± 2 mA.

2.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		2.97	3.3	3.63	V
Device supply voltage CPU, V_{DD}(When internal VREG is disabled)			1.8		V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA}		2.97	3.3	3.63	V
Analog ground, V_{SSA}			0		V
Device clock frequency (system clock)		2		60	MHz
High-level input voltage, V_{IH}(3.3 V)		2		V_{DDIO}	V
High-level input voltage, V_{IH} (1.8 V)		0.7 * V_{DD}			V
Low-Level input voltage, V_{IL} (1.8 V)				0.3 * V_{DD}	V
Low-level input voltage, V_{IL} (3.3 V)				0.8	V

3   Tools and Software Support

The following tools and software are available:

- ANSI C/C++ Compiler/Assembler/Linker
- Code Composer Studio™ IDE
- Digital Motor Control and Digital Power Software Libraries

PRODUCT PREVIEW

KTTIC   http://www.kttic.com

TMS320F2803x and TMS320F2802x MCU Technical Brief

SPRT493−SEPTEMBER 2008

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TEXAS
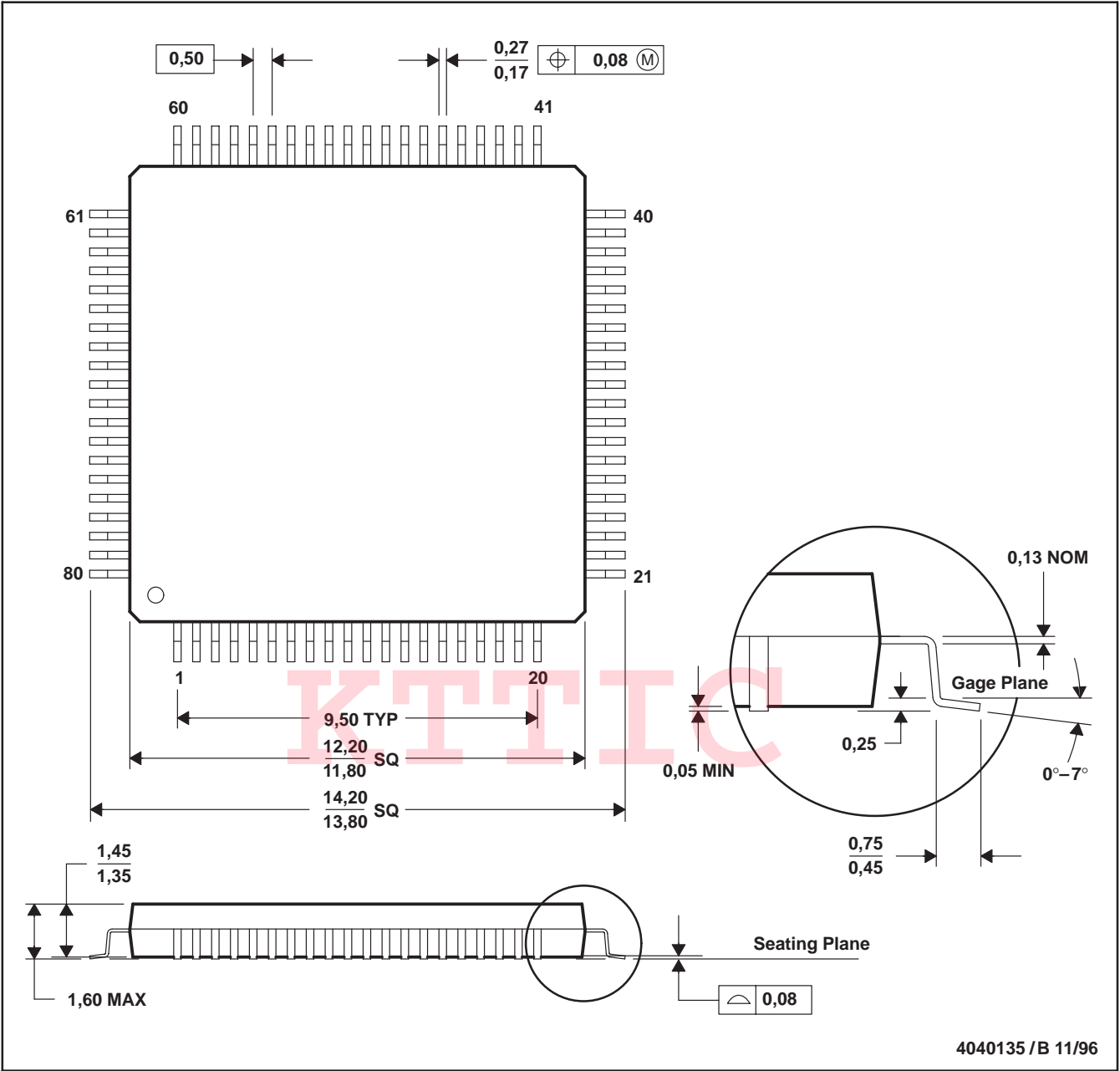INSTRUMENTS

4 Mechanical Data

The mechanical package diagram(s) that follow reflect the most current released mechanical data available for the designated device(s).
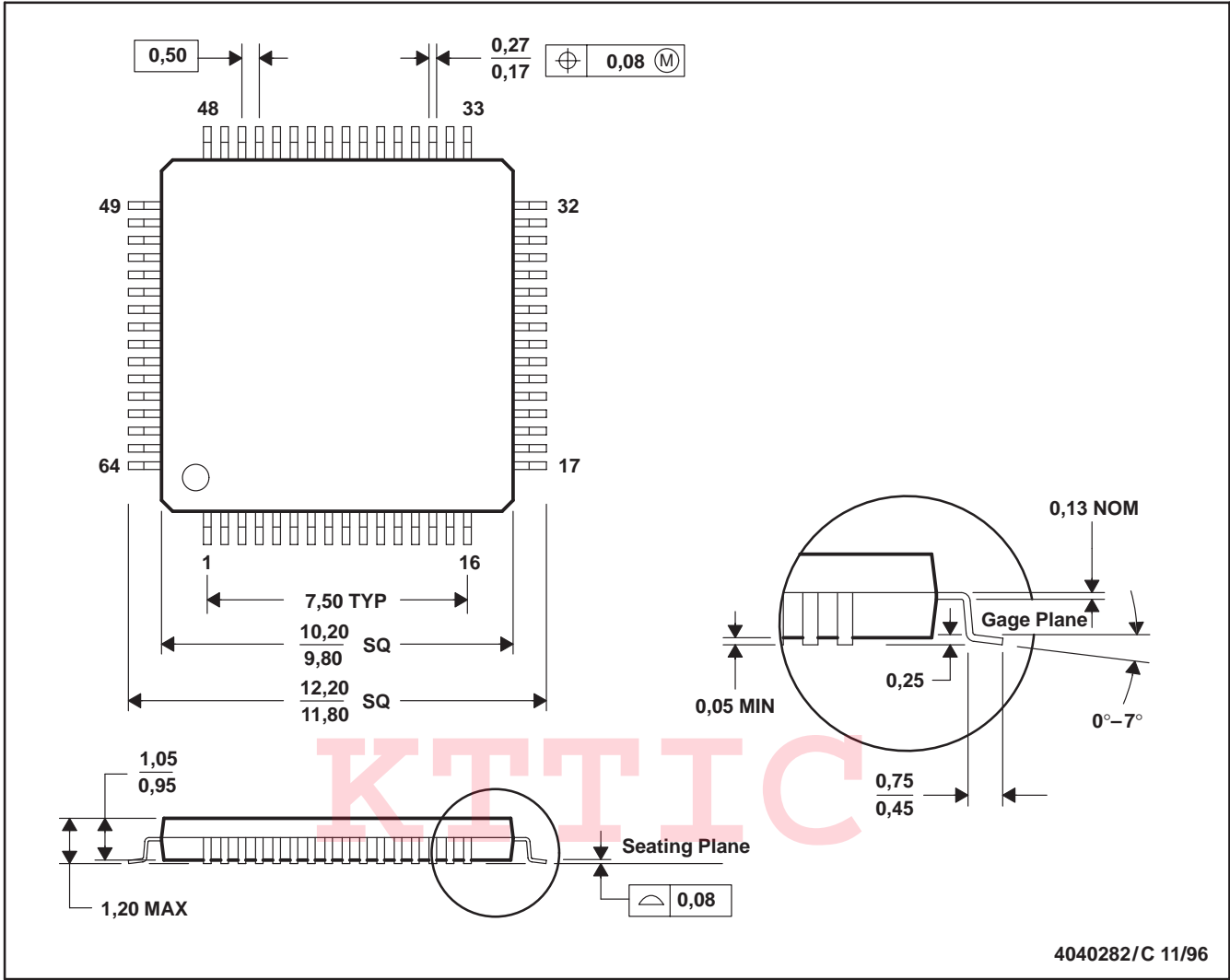
PRODUCT PREVIEW

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80)   **PLASTIC QUAD FLATPACK**

0,50

$\frac{0,27}{0,17}$ ⊕ 0,08 Ⓜ

60   41

61   40

80   21

1   20

9,50 TYP

$\frac{12,20}{11,80}$ SQ

$\frac{14,20}{13,80}$ SQ

0,05 MIN

0,13 NOM

Gage Plane

0,25

0°−7°

$\frac{0,75}{0,45}$
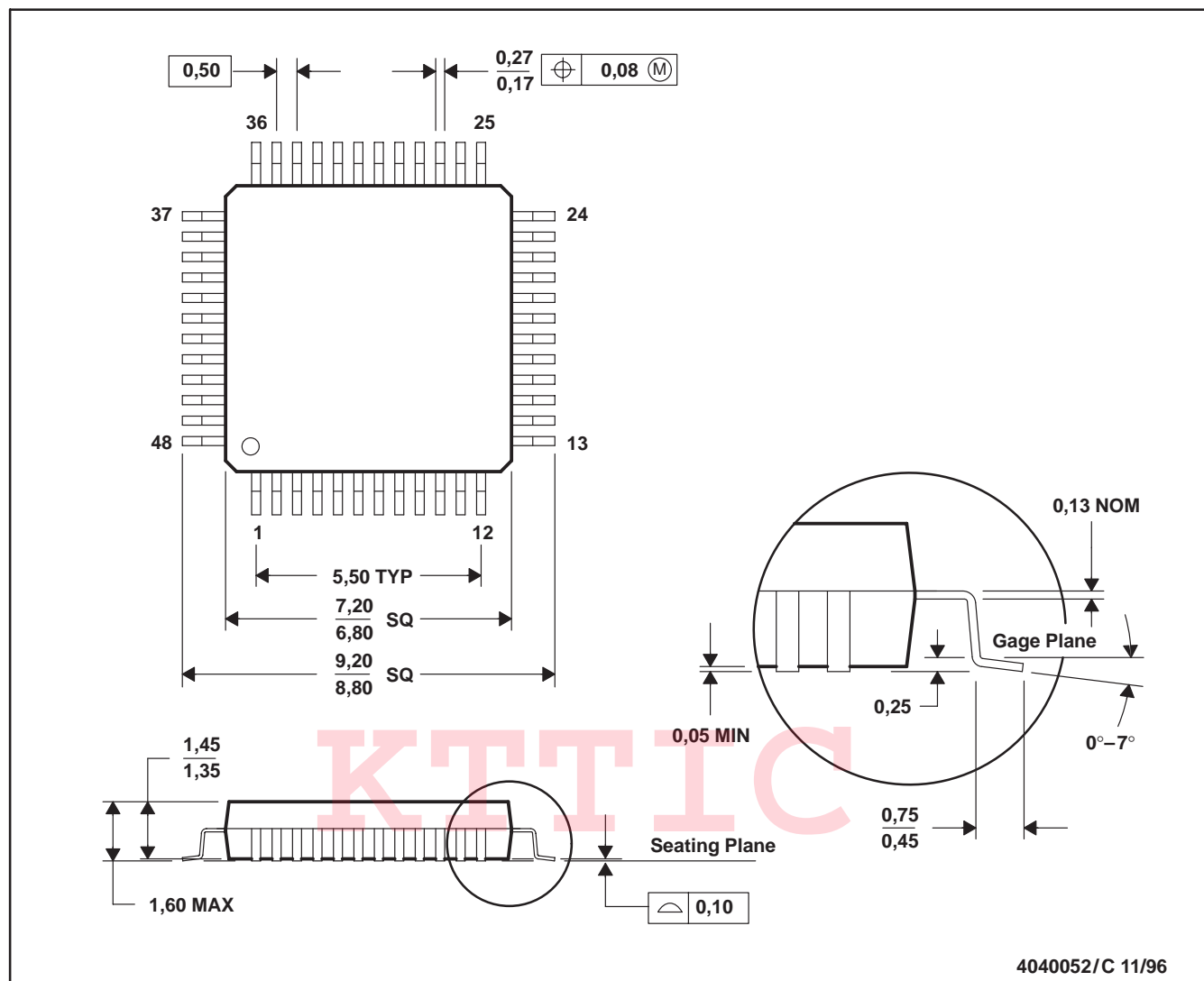
$\frac{1,45}{1,35}$

Seating Plane

1,60 MAX

0,08

4040135 / B 11/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

![TEXAS INSTRUMENTS]

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

MTQF006A – JANUARY 1995 – REVISED DECEMBER 1996

PAG (S-PQFP-G64)   **PLASTIC QUAD FLATPACK**

0,50

$\frac{0,27}{0,17}$ ⊕ 0,08 Ⓜ

48   33

49   32

64   17

0,13 NOM

Gage Plane

1   16

7,50 TYP

$\frac{10,20}{9,80}$ SQ

$\frac{12,20}{11,80}$ SQ

0,25

0,05 MIN

0°−7°

$\frac{1,05}{0,95}$

$\frac{0,75}{0,45}$

Seating Plane

1,20 MAX

△ 0,08

4040282/C 11/96

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS-026

TEXAS INSTRUMENTS
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PT (S-PQFP-G48)　　　　　　　　　　　　　　　　**PLASTIC QUAD FLATPACK**

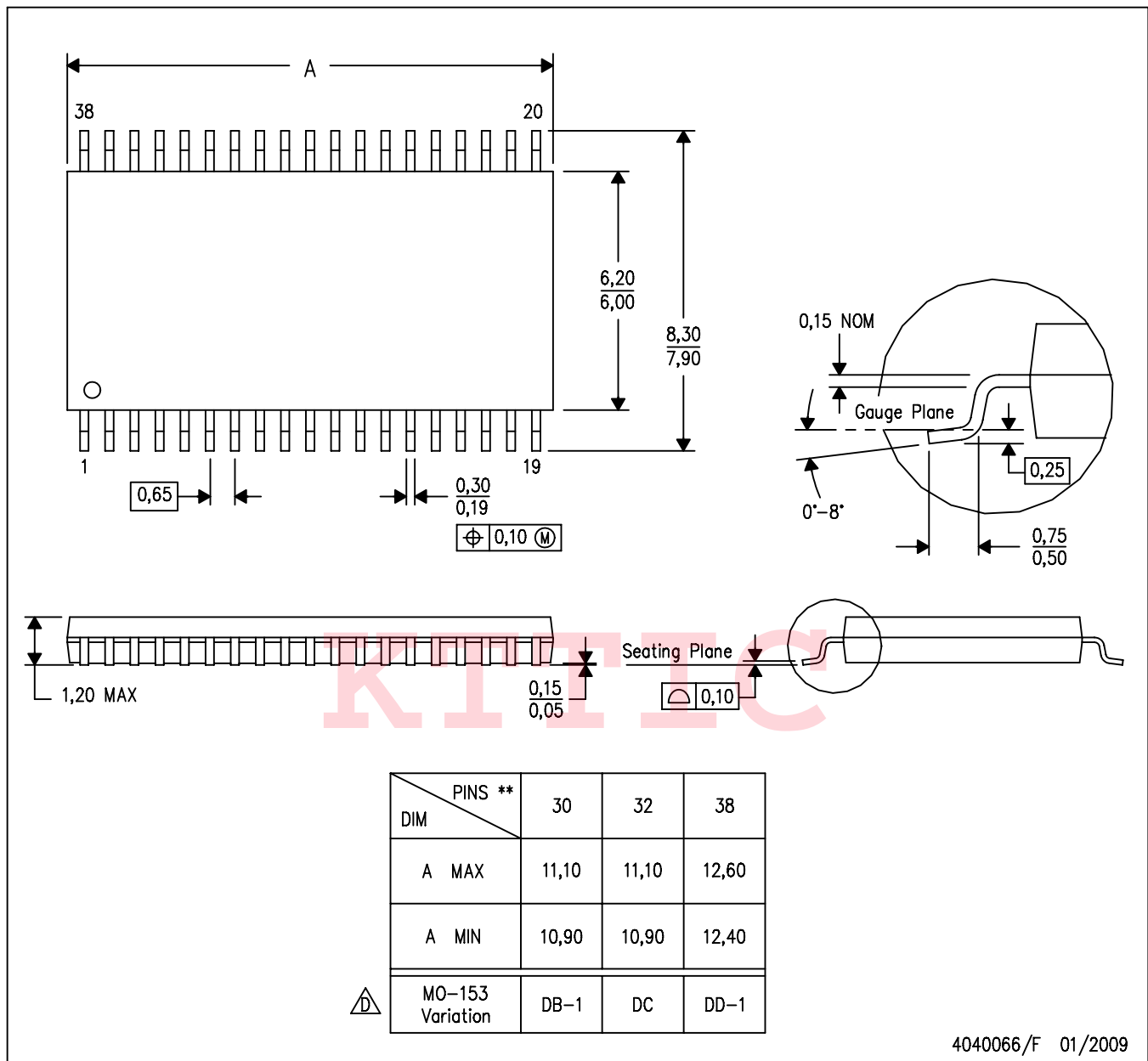

4040052 / C 11/96

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Falls within JEDEC MS-026
　　　　　D.　This may also be a thermally enhanced plastic package with leads conected to the die pads.

DA (R−PDSO−G**)   PLASTIC SMALL−OUTLINE PACKAGE
38 PIN SHOWN

A

38   20

$\dfrac{6,20}{6,00}$

$\dfrac{8,30}{7,90}$

0,15 NOM

Gauge Plane

0°−8°

0,25

$\dfrac{0,75}{0,50}$

1   19

0,65 $\dfrac{0,30}{0,19}$

⊕ 0,10 Ⓜ

1,20 MAX

$\dfrac{0,15}{0,05}$

Seating Plane

◠ 0,10

DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
⚠ MO−153 Variation	DB−1	DC	DD−1

4040066/F   01/2009

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         ⚠ Falls within JEDEC MO−153, except 30 pin body length.

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