SPNS072B – NOVEMBER 2001 – REVISED OCTOBER 2002

- High-Performance Static CMOS Technology
- TMS470R1x 16/32-Bit RISC Core (ARM7TDMI™)
  - 20-MHz System Clock
  - Independent 16/32-Bit Instruction Set
  - Open Architecture With Third-Party Support
  - Built-In Debug Module
  - Utilizes Big-Endian Format
- Upwardly Software-Compatible With the TMS470R1VF336 Device
- Integrated Memory
  - 32K-Byte Program ROM
  - 2.5K-Byte Static RAM (SRAM)
- Operating Features
  - Core Supply Voltage (V_{CC}): 1.8 V Nominal
  - I/O Supply Voltage (V_{CCIO}): 3.3 V Nominal
  - Low-Power Modes: STANDBY and HALT
  - Industrial and Automotive Temperature Ranges
- 470+ System Module
  - 32-Bit Address Space Decoding
  - Bus Supervision for Memory and Peripherals
  - Analog Watchdog (AWD) Timer
  - Real-Time Interrupt (RTI)
  - System Integrity and Failure Detection
- Clock Divider Module (CDM)
  - Crystal Oscillator, Clock Monitor Circuit, and Prescaler
- Serial Peripheral Interface (SPI)
  - 255 Programmable Baud Rates
- 16-Input/Output High-End Timer (HET)
  - 16 Programmable I/O Channels:
    - 12 High-Resolution Pins
    - 4 Standard-Resolution Pins
  - High-Resolution Share Feature (XOR)
  - High-End Timer RAM
    - 32-Instruction Capacity
- Seven External Interrupts
- Flexible Interrupt Handling
- 6 Dedicated GIO Pins,1 Input-Only GIO Pin, and 22 Additional Peripheral I/Os
- On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1† (JTAG) Boundary-Scan Logic
- 100-Pin Plastic Low-Profile Quad Flatpack (PZ Suffix)
- Development System Support Tools Available
  - Code Composer Studio™ IDE
  - HET Assembler and Simulator
  - Real-Time In-Circuit Emulation
- External Clock Prescale (ECP) Module
  - Programmable Low-Frequency External Clock (CLK)

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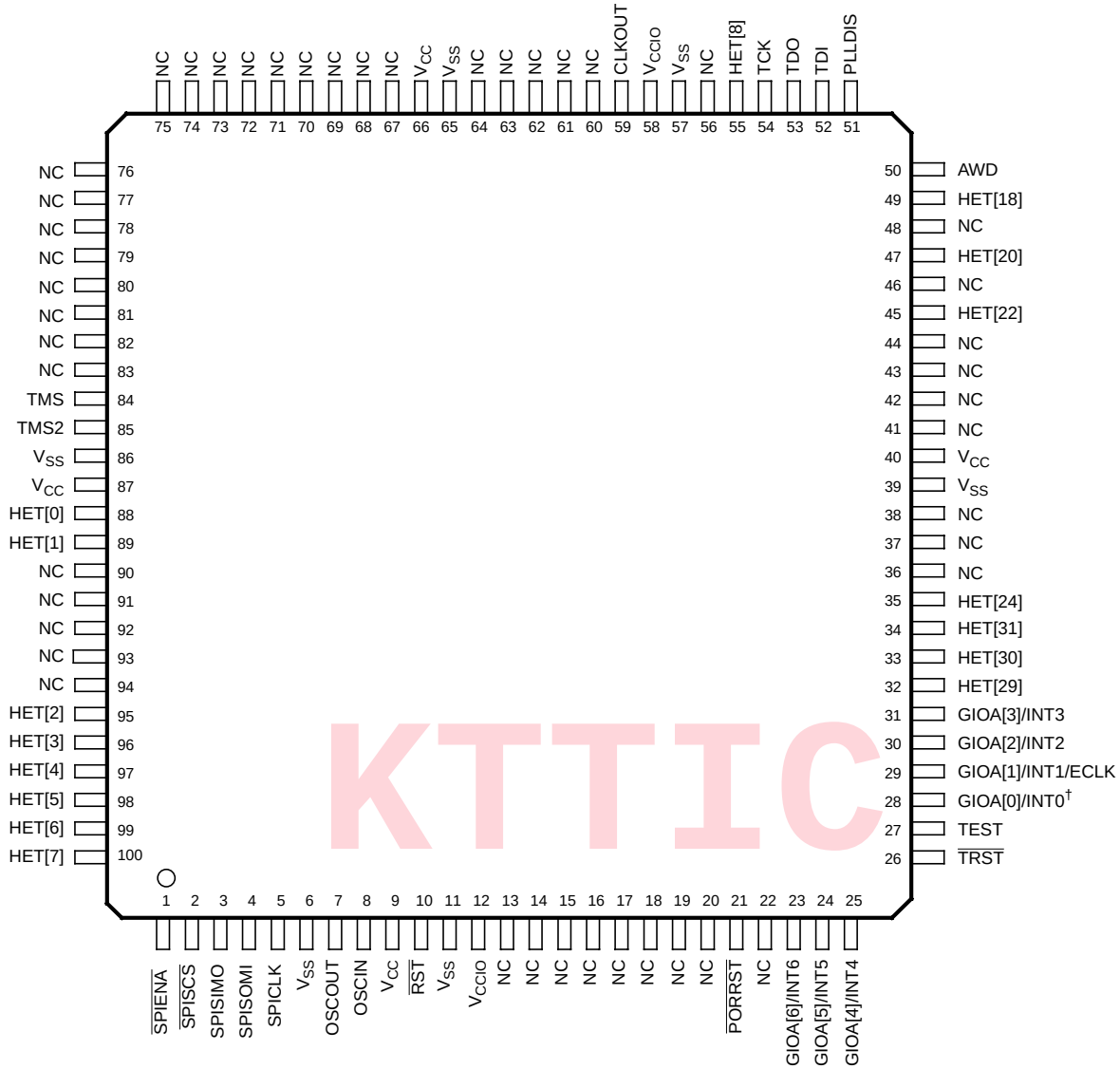
† IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture.

TMS470R1VC002 100-PIN PZ PACKAGE (TOP VIEW)



† GIOA[0]/INT0 (pin 28) is an input-only GIO pin.

description

The TMS470R1VC002† device is a member of the Texas Instruments (TI) TMS470R1x family of general-purpose16/32-bit reduced instruction set computer (RISC) microcontrollers. The VC002 microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from zero. The TMS470R1VC002 utilizes the big-endian format where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The VC002 RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The VC002 device contains the following:

- ARM7TDMI 16/32-Bit RISC CPU
- TMS470R1x system module (SYS) with 470+ enhancements
- 32K-byte ROM
- 2.5K-byte SRAM
- Clock divider module (CDM)
- Analog watchdog (AWD) timer
- Real-time interrupt (RTI) module
- Serial peripheral interface (SPI) module
- High-end timer (HET) controlling 16 I/Os
- External Clock Prescale (ECP)
- Up to 28 I/O pins and 1 input-only pin

The functions performed by the 470+ system module (SYS) include: address decoding; memory and peripherals bus supervision; reset and abort exception management; prioritization for all internal interrupt sources; device clock control; and parallel signature analysis (PSA). This data sheet includes device-specific information such as memory and peripheral select assignment, interrupt priority, and a device memory map. For a more detailed functional description of the SYS module, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

The VC002 memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

The ROM memory on the VC002 device is programmable read-only memory that is masked at the time of device fabrication.

The VC002 device has a serial peripheral interface (SPI). The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. For more detailed functional information on the SPI peripheral, see the *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (literature number SPNU195).

The HET is a 16-bit advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. For more detailed functional information on the HET, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

† The TMS470R1VC002 device name shall be referred to as VC002 throughout the remainder of this document.

description (continued)

The clock divider module (CDM) contains a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1–8). The CDM provides ACLK to the system (SYS) module. The SYS module subsequently provides system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other VC002 device modules. For more detailed functional information on the CDM, see the *TMS470R1x Clock Divider Module (CDM) Reference Guide* (literature number SPNU215).

The VC002 device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock (ECLK) on a specified GIO pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (ICLK) frequency. For more detailed functional information on the ECP, see the *TMS470R1x External Clock Prescaler (ECP) Reference Guide* (literature number SPNU202).

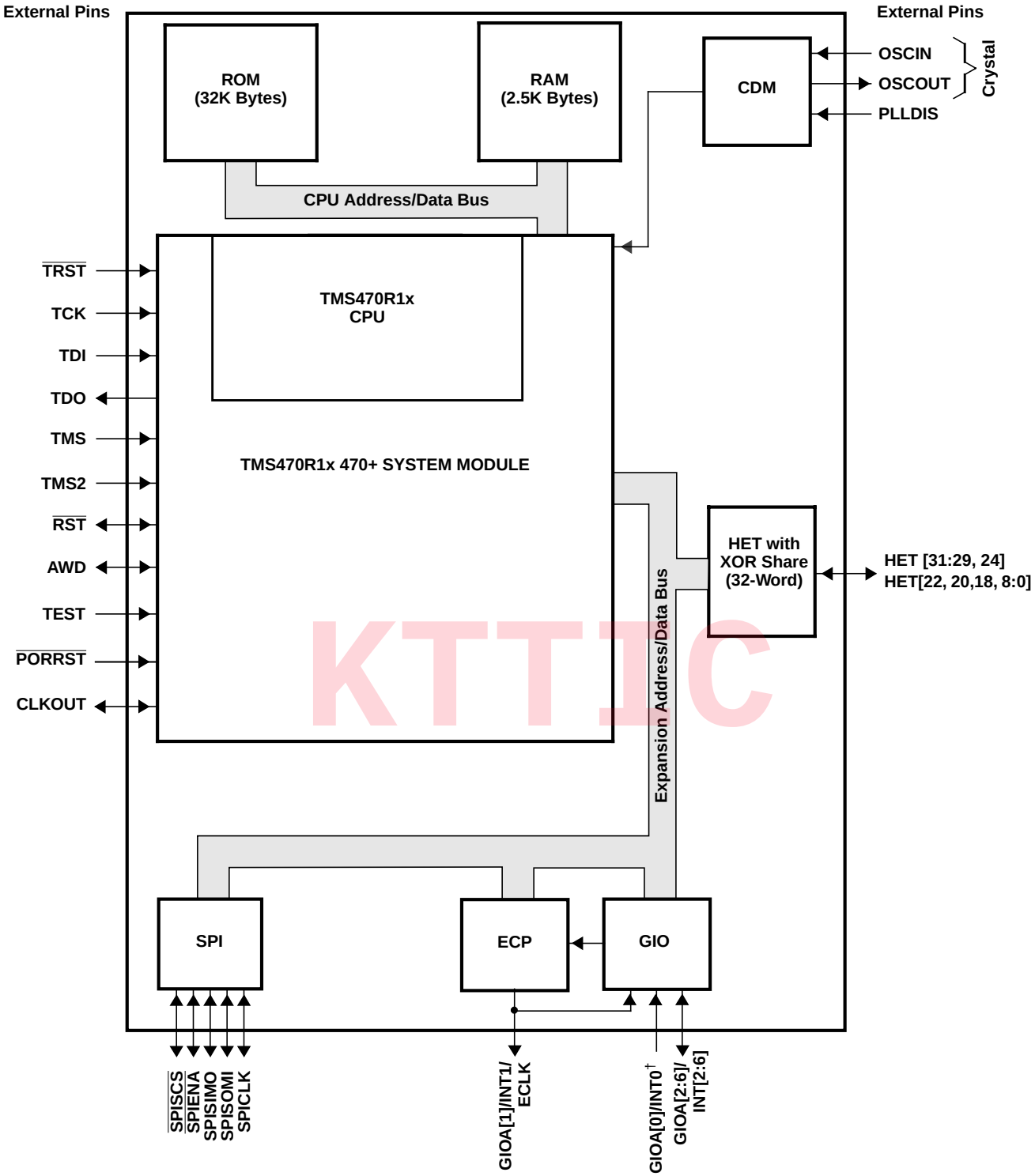
device characteristics

The TMS470R1VC002 device is a derivative of the F05 system emulation device SE470R1VB8AD. Table 1 identifies all the characteristics of the TMS470R1VC002 device except the SYSTEM and CPU, which are generic [the only exception being that the VC002 SYSTEM does *not* support a memory protection unit (MPU). The COMMENTS FOR VC002 column aids the user in software-programming and references device-specific information.

Table 1. Device Characteristics

CHARACTERISTICS	DEVICE DESCRIPTION TMS470R1VC002	COMMENTS FOR VC002
MEMORY		
For the number of memory selects on this device, see the Memory Selection Assignment table (Table 2).		
INTERNAL MEMORY	32K-Byte ROM 2.5K-Byte SRAM	The VC002 RAM is implemented in one 2.5K-byte array selected by two memory-select signals (see the Memory Selection Assignment table, Table 2). The VC002 SYSTEM module does *not* support a memory protection unit (MPU).
PERIPHERALS		
For the device-specific interrupt priority configurations, see the Interrupt Priority table (Table 4). And for the 1K peripheral address ranges and their peripheral selects, see the VC002 Peripherals and System Module Addresses table (Table 3).		
CLOCK	CDM	The clock divider module (CDM) has no PLL, and therefore, no multiply factors for the clock.
GENERAL-PURPOSE I/Os	6 I/O 1 Input only	Port A has only seven (7) external pins (GIOA[7]/INT7 is not applicable)
ECP	YES	The ECP uses the GIOA[1]/INT1/ECLK pin
SPI (5-pin, 4-pin or 3-pin)	1 (5-pin)	SPI (5-pin)
HET with XOR Share	16 I/O	The VC002 has both the logic and registers for a 16-I/O HET. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET RAM	32-Instruction Capacity	
CORE VOLTAGE	1.8 V	
I/O VOLTAGE	3.3 V	
PINS	100	
PACKAGE	PZ	

functional block diagram



† GIOA[0]/INT0 is an input-only GIO pin.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
HIGH-END TIMER (HET)				
HET[0]	88	3.3-V I/O	IPD	The VC002 has both the logic and registers for a 16-I/O HET. Timer input capture or output compare. The HET[31:0] applicable pins can be programmed as general-purpose input/output (GIO) pins. HET[22, 20, 18, 8:0] are high-resolution pins and HET[31:29, 24] are standard-resolution pins. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET[1]	89			
HET[2]	95			
HET[3]	96			
HET[4]	97			
HET[5]	98			
HET[6]	99			
HET[7]	100			
HET[8]	55			
HET[18]	49			
HET[20]	47			
HET[22]	45			
HET[24]	35			
HET[29]	32			
HET[30]	33			
HET[31]	34			
GENERAL-PURPOSE I/O (GIO)				
GIOA[0]/INT0	28	3.3-V I	IPD	General-purpose input/output pins. GIOA[0]/INT0 is an input-only pin. GIOA[6:0]/ INT[6:0] are interrupt-capable pins. The GIOA[1]/INT1/ECLK pin is multiplexed with the external clock-out function of the external clock prescale (ECP) module.
GIOA[1]/INT1/ ECLK	29	3.3-V I/O		
GIOA[2]/INT2	30			
GIOA[3]/INT3	31			
GIOA[4]/INT4	25			
GIOA[5]/INT5	24			
GIOA[6]/INT6	23			
SERIAL PERIPHERAL INTERFACE (SPI)				
SPICLK	5	3.3-V I/O	IPD	SPI clock. SPICLK can be programmed as a GIO pin.
$\overline{\text{SPIENA}}$	1			SPI chip enable. $\overline{\text{SPIENA}}$ can be programmed as a GIO pin.
$\overline{\text{SPISCS}}$	2			SPI slave chip select. $\overline{\text{SPISCS}}$ can be programmed as a GIO pin.
SPISIMO	3			SPI data stream. Slave in/master out. SPISIMO can be programmed as a GIO pin.
SPISOMI	4			SPI data stream. Slave out/master in. SPISOMI can be programmed as a GIO pin.
CLOCK DIVIDER MODULE (CDM)				
OSCIN	8	1.8-V I		Crystal connection pin or external clock input
OSCOUT	7	1.8-V O		External crystal connection pin
PLLDIS	51	3.3-V I	IPD	This pin is required for test purposes only. The Clock-Divider Module (CDM) on the VC002 device does not support a PLL circuit. When PLLDIS is high, the 4 096-cycle clock counter is disabled.

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect
‡ All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
SYSTEM MODULE (SYS)				
CLKOUT	59	3.3-V I/O	IPD	Bidirectional pin. CLKOUT can be programmed as a GIO pin or the output of SYSCLK, ICLK, or MCLK. Note: If this pin is to be used as an input, it is recommended that an external pulldown be used.
$\overline{\text{PORRST}}$	21	3.3-V I	IPD	Input master chip power-up reset. External V_{CC} monitor circuitry must assert a power-on reset.
$\overline{\text{RST}}$	10	3.3-V I/O	IPU	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On this pin, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin.
WATCHDOG/REAL-TIME INTERRUPT (WD/RTI)				
AWD	50	3.3-V I/O	IPD	Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. For more details on the external RC network circuit, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).
TEST/DEBUG (T/D)				
TCK	54	3.3-V I	IPD	Test clock. TCK controls the test hardware (JTAG).
TDI	52	3.3-V I	IPU	Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG).
TDO	53	3.3-V O	IPD	Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG).
TEST	27	3.3-V I	IPD	Test enable. Reserved for internal use only. **For proper operation, this pin must be connected to ground.**
TMS	84	3.3-V I	IPU	Serial input for controlling the state of the CPU TAP controller (JTAG)
TMS2	85	3.3-V I	IPU	Serial input for controlling the second TAP. **For proper operation, this pin must be connected to V_{CC} or not connected.**
$\overline{\text{TRST}}$	26	3.3-V I	IPD	Test hardware reset to TAP1 and TAP2. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic **For proper device operation, the $\overline{\text{TRST}}$ pin must be externally pulled down with a 10-kΩ resistor.**
SUPPLY VOLTAGE CORE (1.8 V)				
V_{CC}	9 40 66 87	1.8-V PWR		Core logic supply voltage
SUPPLY VOLTAGE DIGITAL I/O (3.3 V)				
V_{CCIO}	12 58	3.3-V PWR		Digital I/O supply voltage

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect
‡ All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
SUPPLY GROUND				
V_{SS}	6	GND		Supply ground reference
	11			
	39			
	57			
	65			
	86			
NO CONNECTS				
NC	13	NC		No Connection
	14			
	15			
	16			
	17			
	18			
	19			
	20			
	22			
	36			
	37			
	38			
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† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect
‡ All I/O pins, except $\overline{RST}$, are configured as inputs while $\overline{PORRST}$ is low and immediately after $\overline{PORRST}$ goes high.
§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{PORRST}$ state.)

Terminal Functions (Continued)

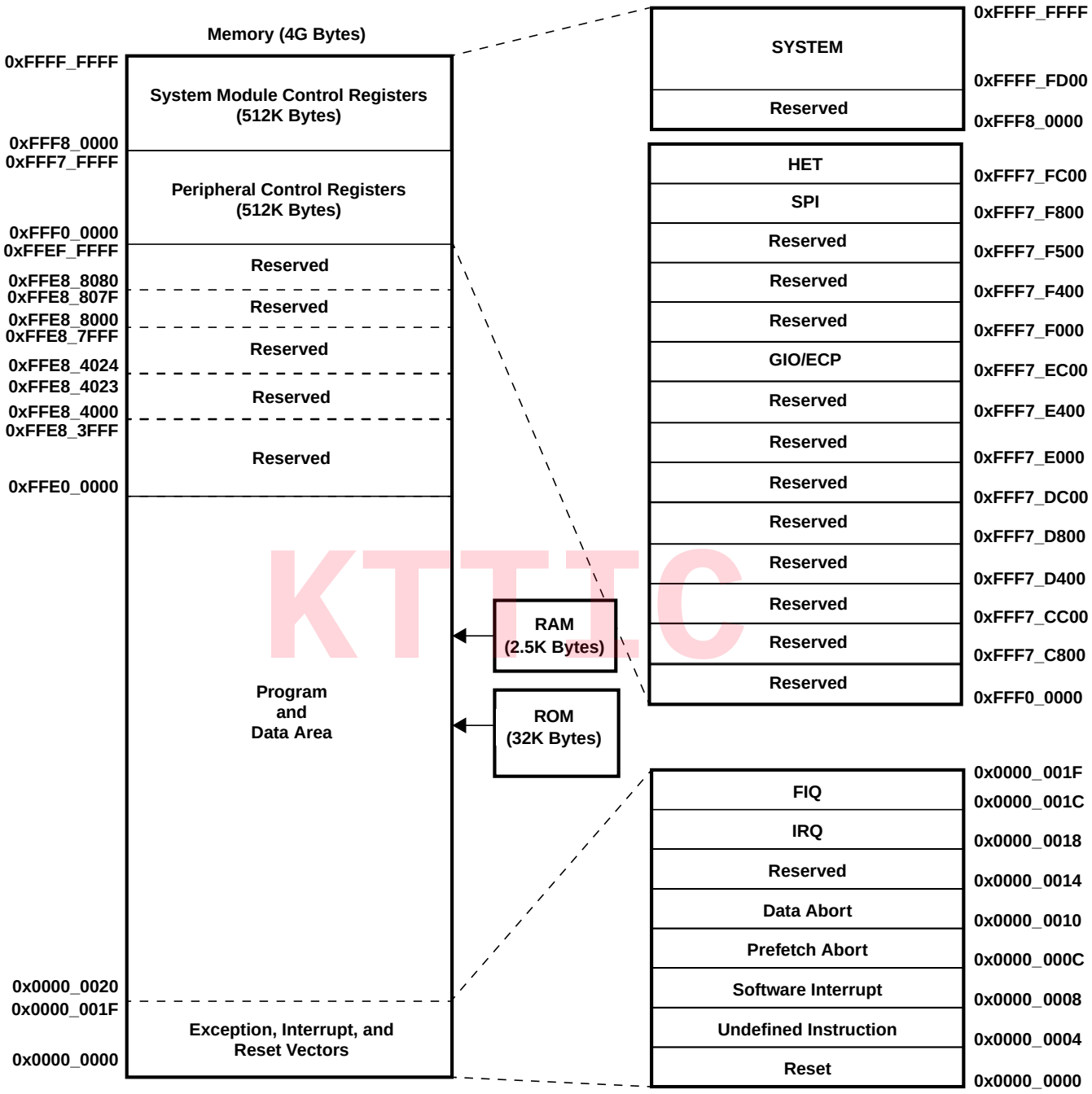
TERMINAL NAME	TERMINAL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
NO CONNECTS (CONTINUED)				
NC	78	NC		No Connection
	79			
	80			
	81			
	82			
	83			
	90			
	91			
	92			
	93			
	94			

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect
‡ All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

VC002 DEVICE-SPECIFIC INFORMATION

memory

Figure 1 shows the memory map of the VC002 device.



NOTES: A. Memory addresses are configurable by the system (SYS) module within the range of 0x0000_0000 to 0xFFE0_0000.
B. The CPU registers are not a part of the memory map.

Figure 1. Memory Map

memory selects

Memory selects allow the user to address memory arrays (i.e., ROM, RAM, and HET RAM) at user-defined addresses. Each memory select has its own set (low and high) of memory base address registers (MFBAHRx and MFBALRx) that, together, define the array's starting (base) address, block size, and protection.

The base address of each memory select is configurable to any memory address boundary that is a multiple of the decoded block size. For more information on how to control and configure these memory select registers, see the bus structure and memory sections of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

For the memory selection assignments and the memory selected, see Table 2.

Table 2. Memory Selection Assignment

MEMORY SELECT	MEMORY SELECTED (ALL INTERNAL)	MEMORY SIZE	MPU	MEMORY BASE ADDRESS REGISTER	STATIC MEM CTL REGISTER
0 (fine)	ROM	32K	NO	MFBAHR0 and MFBALR0	
1 (fine)	ROM		NO	MFBAHR1 and MFBALR1	
2 (fine)	RAM	2.5K†	NO	MFBAHR2 and MFBALR2	
3 (fine)	RAM		NO	MFBAHR3 and MFBALR3	
4 (fine)	HET RAM	1K		MFBAHR4 and MFBALR4	SMCR1

† The starting addresses for both RAM memory-select signals *cannot* be offset from each other by a multiple of the user-defined block size in the memory-base address register. There is no illegal address detection for RAM accesses between 2.5 K and 3.0 K bytes.

RAM

The VC002 device contains 2.5K bytes of internal static RAM configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. This VC002 RAM is implemented in one 2.5K-byte array selected by two memory-select signals. This VC002 configuration imposes an additional constraint on the memory map for RAM; the starting addresses for both RAM memory selects *cannot* be offset from each other by the multiples of the size of the physical RAM (i.e., 2.5K for the VC002 device). The VC002 RAM is addressed through memory selects 2 and 3.

ROM

The program ROM consists of 32K bytes mask programmable read-only memory. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication.

HET RAM

The VC002 device contains HET RAM. The HET RAM has a 32-instruction capability. The HET RAM is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The HET RAM is addressed through memory select 4.

memory protection (not available on VC002)

This VC002 device has no memory protection unit (MPU) in the 470+ SYS module; therefore, this device does *not* support memory protection for the RAM and ROM (see Table 2).

XOR share

The VC002 HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high-resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET. For more detailed information on the HET XOR-share feature, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

peripheral selects and base addresses

The VC002 device uses three of the sixteen peripheral selects to decode the base addresses of the peripherals. These peripheral selects are fixed and transparent to the user since they are part of the decoding scheme used by the SYS module.

Control registers for the peripherals and SYS module begin at the base addresses shown in Table 3.

Table 3. VC002 Peripherals and System Module Addresses

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
SYSTEM	0XFFFF_FD00	0XFFFF_FFFF	N/A
RESERVED	0XFFF8_0000	0XFFFF_FCFF	N/A
HET	0XFFF7_FC00	0XFFF7_FFFF	PS[0]
SPI	0XFFF7_F800	0XFFF7_FBFF	PS[1]
RESERVED	0XFFF7_F500	0XFFF7_F7FF	PS[2]
RESERVED	0XFFF7_F400	0XFFF7_F4FF	
RESERVED	0XFFF7_F000	0XFFF7_F3FF	PS[3]
GIO/ECP	0XFFF7_EC00	0XFFF7_EFFF	PS[4]
RESERVED	0XFFF7_E400	0XFFF7_EBFF	PS[5] - PS[6]
RESERVED	0XFFF7_E000	0XFFF7_E3FF	PS[7]
RESERVED	0XFFF7_DC00	0XFFF7_DFFF	PS[8]
RESERVED	0XFFF7_D800	0XFFF7_DBFF	PS[9]
RESERVED	0XFFF7_D400	0XFFF7_D7FF	PS[10]
RESERVED	0XFFF7_CC00	0XFFF7_D3FF	PS[11] - PS[12]
RESERVED	0XFFF7_C800	0XFFF7_CBFF	PS[13]
RESERVED	0XFFF7_C000	0XFFF7_C7FF	PS[14] - PS[15]
RESERVED	0XFFF0_0000	0XFFF7_BFFF	N/A
RESERVED	0XFFE8_8000	0XFFE8_807F	N/A
RESERVED	0XFFE8_4000	0XFFE8_4023	N/A

interrupt priority

The central interrupt manager (CIM) portion of the SYS module manages the interrupt requests from the device modules (i.e., SPI, HET, and RTI, etc.).

Although the CIM can accept up to 32 interrupt request signals, the VC002 device only uses 9 of those interrupt request signals. The request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the CIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The precedences of request channels decrease with ascending channel order in the CIM (0 [highest] and 31 [lowest] priority). For these channel priorities and the associated modules, see Table 4.

Table 4. Interrupt Priority

MODULES	INTERRUPT SOURCES	INTERRUPT LEVEL/CHANNEL
SPI	SPI end-transfer/overrun	0
RTI	COMP2 interrupt	1
RTI	COMP1 interrupt	2
RTI	TAP interrupt	3
Reserved		4
GIO	Interrupt A	5
Reserved		6
HET	Interrupt 1	7
Reserved		8
Reserved		9
Reserved		10
Reserved		11
Reserved		12
Reserved		13
Reserved		14
Reserved		15
Reserved		16
Reserved		17
Reserved		18
Reserved		19
Reserved		20
System	SW interrupt (SSI)	21
Reserved		22
HET	Interrupt 2	23
Reserved		24
Reserved		25
Reserved		26
Reserved		27
Reserved		28
GIO	Interrupt B	29
Reserved		30
Reserved		31

development system support

Texas Instruments provides extensive hardware and software development support tools for the TMS470R1x family. These support tools include:

- Code Composer Studio™ IDE
  - Fully integrated suite of software development tools
  - Includes Compiler/Assembler/Linker, Debugger, and Simulator
  - Supports Real-Time analysis, data visualization, and open API
- Optimizing C compiler
  - Supports high-level language programming
  - Full implementation of the standard ANSI C language
  - Powerful optimizer that improves code-execution speed and reduces code size
  - Extensive run-time support library included
  - TMS470R1x control registers easily accessible from the C program
  - Interfaces C functions and assembly functions easily
  - Establishes comprehensive, easy-to-use tool set for the development of high-performance microcontroller applications in C/C++
- Assembly language tools (assembler and linker)
  - Provides extensive macro capability
  - Allows high-speed operation
  - Allows extensive control of the assembly process using assembler directives
  - Automatically resolves memory references as C and assembly modules are combined
- TMS470R1x CPU Simulator
  - Provides capability to simulate CPU operation without emulation hardware
  - Allows inspection and modifications of memory locations
  - Allows debugging programs in C or assembly language
- XDS510™ emulation communication kit
  - Allows high-speed JTAG communication to the TMS470R1x emulator or target board
  - Includes XDS510 ISA PC card and JTAG emulation cable
- XDS510WS™ emulation communication kit
  - Allows high-speed JTAG communication to the TMS470R1x emulator or target board
  - Includes XDS510 Workstation communication box and JTAG emulation cable
- XDS510PP™ emulation communication kit
  - Allows JTAG communication to the TMS470R1x emulator or target board with a connection to the PC parallel port
  - Includes XDS510PP communication box and parallel port cable
- XDS560™ emulator
  - Allows high-speed JTAG communication to the TMS470R1x emulator or target board
  - Includes XDS560 communication board and cable

Code Composer Studio, XDS510, XDS510WS, XDS510PP, and XDS560 are trademarks of Texas Instruments.

development system support (continued)

Table 5, Table 6, and Table 7 provide the part numbers for the TMS470R1VC002 hardware and software development tools.

Table 5. Code Development Tools

PRODUCT	DESCRIPTION	HOST	OPERATING SYSTEM
TMDX474A596-07	C/C++ Compiler Assembler/Linker	SPARC™, HP™	SunOS™ 5.5 HP-UX™ 10.2 Solaris™ 2.5
TMDX474H852-02	HET Assembler/Simulator	PC™, SPARC, HP	MS-DOS™ Windows™ 95 Windows 98 Windows NT™ SunOS 4.1.3 HP-UX 9.0.3

Table 6. Debug Tools

PRODUCT	DESCRIPTION	HOST	OPERATING SYSTEM
TMDS474785F-07	Code Composer Studio™ IDE	PC	Windows 95 Windows 98 Windows NT
TMDS4740551-07	SW Simulator	SPARC, HP	SunOS 4.1.3 HP-UX 9.0x Solaris 2.x
TMDX4740600	Emulation SW Kit XDS510WS™ Debugger	SPARC, HP	SunOS 5.5x HP-UX 10.2x Solaris 2.5x

Table 7. Hardware Tools

PRODUCT	DESCRIPTION	HOST	OPERATING SYSTEM
TMDS00510	XDS510™ Board JTAG Controller Kit Emulator Cable	PC (ISA)	Windows 95 Windows 98 Windows NT
TMDS00510WS	XDS510WS™ Box JTAG Controller Kit Emulator Cable	SPARC, HP	SunOS 4.1.x HP-UX 9.0x
TMDS3P701014	XDS510™ Parallel Port JTAG System Kit	PC	Windows 95 Windows 98 Windows NT

Note: Additional hardware and software development tools are available directly from ARM Ltd.
PC is a trademark of International Business Machines Corporation.
MS-DOS, Windows, and Windows NT are registered trademarks of Microsoft Corp.
SPARC is a trademark of SPARC International, Inc.
HP and HP-UX are trademarks of Hewlett-Packard Company.
SunOS and Solaris are trademarks of Sun Microsystems, Inc.

device numbering conventions

Figure 2 illustrates the numbering and symbol nomenclature for the TMS470R1x family.

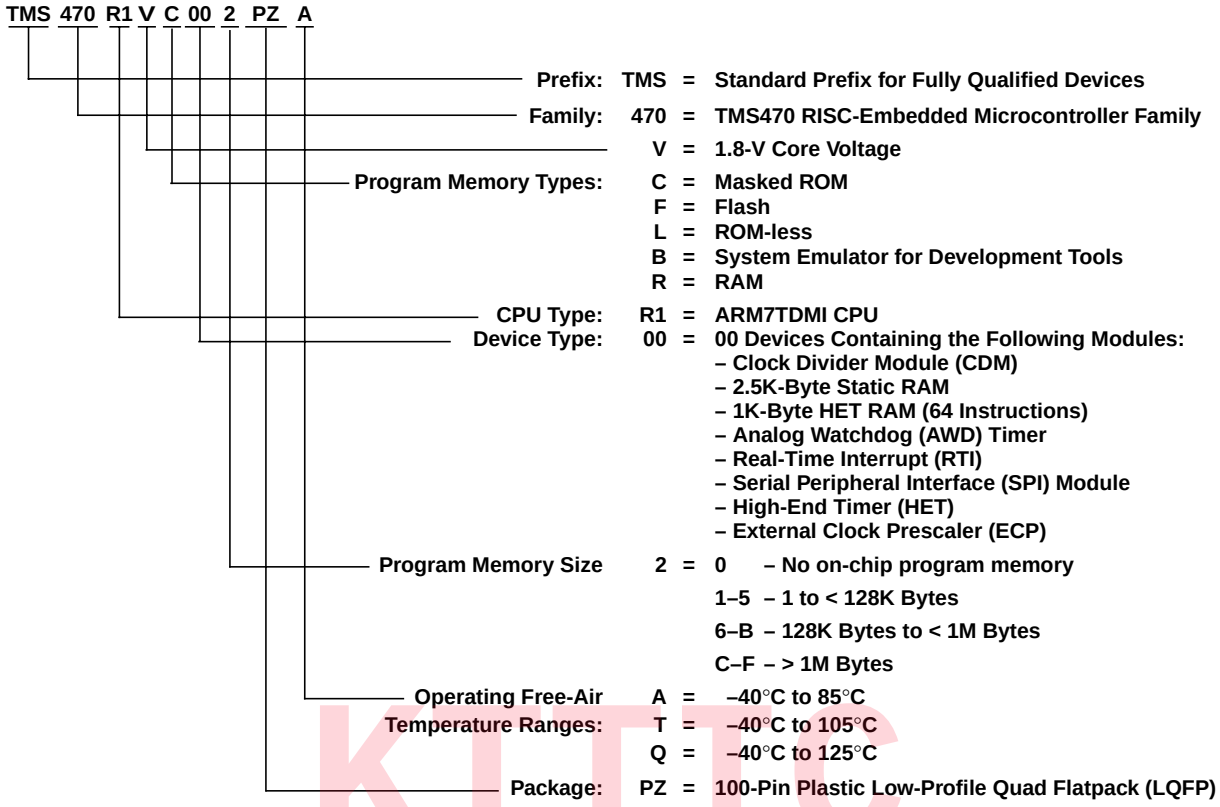


Figure 2. TMS470R1x Family Nomenclature

device identification code register

The device identification code register identifies the silicon version, the technology family (TF), a ROM or Flash device, and an assigned device-specific part number (see Table 8). The VC002 device identification code register value is 0x0C47.

Table 8. TMS470 Device ID Bit Allocation Register

	BIT 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	BIT 16
FFFF_FFF0	Reserved															
	R-0															

	BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
	0	VERSION			TF	R/F	PART NUMBER							1	1	1
	R-0	R-K			R-K	R-K	R-K							R-1	R-1	R-1

LEGEND:
For bit 15: R = Read only, -0 = Value after $\overline{\text{RST}}$
For bits 3–14: R = Read only, -K = Value constant after $\overline{\text{RST}}$
For bits 0–2: R = Read only, -1 = Value after $\overline{\text{RST}}$

Bits 31:16 **Reserved.** Reads are undefined and writes have no effect.

Bit 15 **"0" Mandatory Low.** Bit 15 is tied low by default.

Bits 14:12 **VERSION.** Silicon version (revision) bits

These bits identify what version of silicon the device is. Initial device version numbers start at "000".

Bit 11 **TF.** Technology Family (TF) bit

This bit distinguishes the technology family core power supply:

0 = 3.3 V for F10/C10 devices

1 = 1.8 V for F05/C05 devices

Bit 10 **R/F.** ROM/Flash bit

This bit distinguishes between ROM and Flash devices:

0 = Flash device

1 = ROM device

Bits 9:3 **PART NUMBER.** Device-specific part number bits

These bits identify the assigned device-specific part number.

The assigned device-specific part number for the VC002 device is: 0001000.

Bits 2:0 **"1" Mandatory High.** Bits 2,1, and 0 are tied high by default.

device part numbers

Table 9 lists all the available TMS470R1VC002 devices.

Table 9. Device Part Number

DEVICE PART NUMBER	PROGRAM MEMORY		PACKAGE TYPE	TEMPERATURE RANGES		
	ROM	FLASH EEPROM	100-PIN LQFP	–40°C TO 85°C	–40°C TO 105°C	–40°C TO 125°C
TMS470R1VC002PZA	X		X	X		
TMS470R1VC002PZT	X		X		X	
TMS470R1VC002PZQ	X		X			X

DEVICE ELECTRICAL SPECIFICATIONS AND TIMING PARAMETERS

absolute maximum ratings over operating free-air temperature range, Q version (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 2.5 V
Supply voltage range, V_{CCIO} (see Note 1) . . . . . –0.3 V to 4.1V
Input voltage range: All input pins. . . . . –0.3 V to 4.1 V
Input clamp current: I_{IK} ($V_I < 0$ or $V_I > V_{CCIO}$)
All pins except $\overline{PORRST}$, $\overline{TRST}$, TEST, and TCK . . . . . ±20 mA
Operating free-air temperature ranges, T_A: A version . . . . . –40°C to 85°C
T version . . . . . –40°C to 105°C
Q version . . . . . –40°C to 125°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to their associated grounds.

device recommended operating conditions‡

			MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)		1.71		2.05	V
V_{CCIO}	Digital logic supply voltage (I/O)		3	3.3	3.6	V
V_{SS}	Digital logic supply ground			0		V
T_A	Operating free-air temperature	A version	– 40		85	°C
		T version	– 40		105	°C
		Q version	– 40		125	°C
T_J	Operating junction temperature		– 40		150	°C

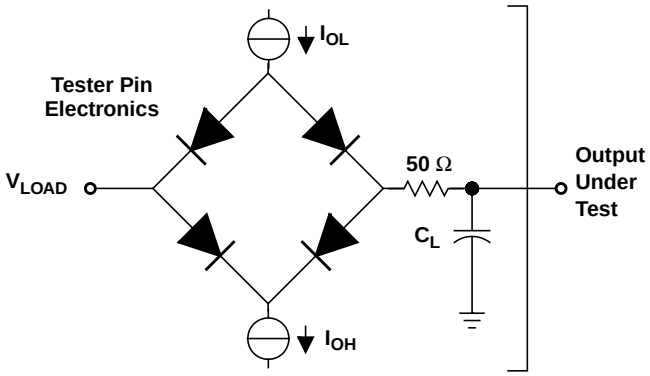
‡ All voltages are with respect to V_{SS}.

electrical characteristics over recommended operating free-air temperature range, Q version (unless otherwise noted)†

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis			0.15			V
V_{IL}	Low-level input voltage	All inputs‡		– 0.3		0.8	V
V_{IH}	High-level input voltage	All inputs		2		V_{CCIO} + 0.3	V
V_{th}	Input threshold voltage	AWD only		1.3		1.7	V
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.2 V_{CCIO}	V
			I_{OL} = 50 µA			0.2	
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	0.8 V_{CCIO}			V
			I_{OH} = 50 µA	V_{CCIO} – 0.2			
I_{IC}	Input clamp current (I/O pins)§		$V_I < V_{SSIO} - 0.3$ or $V_I > V_{CCIO} + 0.3$	–1		1	mA
I_I	Input current (I/O pins)	I_{IL} Pulldown	$V_I = V_{SS}$	–1		1	µA
		I_{IH} Pulldown	$V_I = V_{CC}$	5		40	
		I_{IL} Pullup	$V_I = V_{SS}$	–40		–5	
		I_{IH} Pullup	$V_I = V_{CC}$	–1		1	
		All other pins	No pullup or pulldown	–1		1	
I_{OL}	Low-level output current	CLKOUT, AWD, TDO	V_{OL} = V_{OL} MAX			8	mA
		$\overline{RST}$	V_{OL} = V_{OL} MAX			4	
		All other output pins	V_{OL} = V_{OL} MAX			2	
I_{OH}	High-level output current	CLKOUT, AWD, TDO	V_{OH} = V_{OH} MIN	–8			mA
		All other output pins except $\overline{RST}$	V_{OH} = V_{OH} MIN	–2			
C_I	Input capacitance				2		pF
C_O	Output capacitance				3		pF
I_{CC}	V_{CC} Digital supply current (operating mode)		SYSCLK = 20 MHz, ICLK = 10 MHz, V_{CC} = 2.05 V			30	mA
	V_{CC} Digital supply current (standby mode)		OCSIN = 5 MHz, V_{CC} = 2.05 V			1.0	mA
	V_{CC} Digital supply current (halt mode)		All frequencies, V_{CC} = 2.05 V			200	µA
I_{CCIO}	V_{CCIO} Digital supply current (operating mode)		No DC load, V_{CCIO} = 3.6 V¶			10	mA
	V_{CCIO} Digital supply current (standby mode)		No DC load, V_{CCIO} = 3.6 V¶			100	µA
	V_{CCIO} Digital supply current (halt mode)		No DC load, V_{CCIO} = 3.6 V¶			20	µA

† Source currents (out of the device) are negative while sink currents (into the device) are positive.
‡ This does not apply to the $\overline{PORRST}$ pin. For $\overline{PORRST}$ exceptions, see the $\overline{RST}$ and $\overline{PORRST}$ timings section on page 27.
§ This parameter does not apply to input-only or output-only pins.
¶ I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} – 0.2 V.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = I_{OL} MAX for the respective pin (see Note A)
I_{OH} = I_{OH} MIN for the respective pin (see Note A)
V_{LOAD} = 1.5 V
C_L = 150-pF typical load-circuit capacitance (see Note B)

NOTES: A. For these values, see the electrical characteristics over recommended operating free-air temperature range table.
B. All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

Figure 3. Test Load Circuit

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

CM	Compaction, CMPCT	RD	Read
CO	CLKOUT	RST	Reset, $\overline{\text{RST}}$
ER	Erase	S	Slave mode
ICLK	Interface clock	SIMO	SPInSIMO
M	Master mode	SOMI	SPInSOMI
OSC, OSCI	OSCIN	SPC	SPInCLK
OSCO	OSCOUT	SYS	System clock
P	Program, PROG		
R	Ready		
R0	Read margin 0, RDMRGN0		
R1	Read margin 1, RDMRGN1		

Lowercase subscripts and their meanings are:

a	access time	r	rise time
c	cycle time (period)	su	setup time
d	delay time	t	transition time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

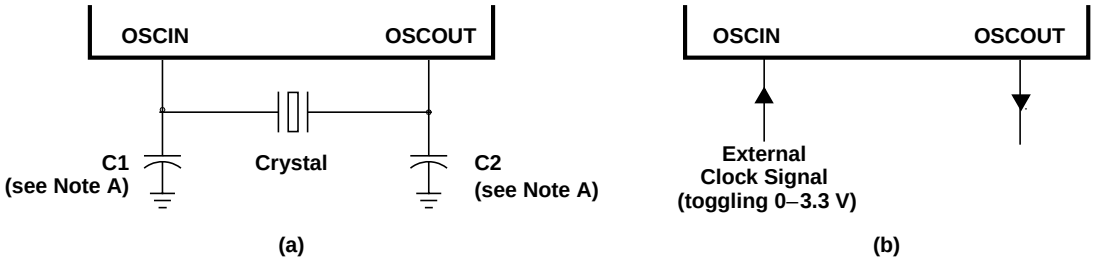
The following additional letters are used with these meanings:

H	High	X	Unknown, changing, or don't care level
L	Low	Z	High impedance
V	Valid		

external reference resonator/crystal oscillator clock option

The oscillator is enabled by connecting the appropriate fundamental 4–20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 4a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a TTL- or CMOS-level clock signal to the OSCIN pin and leaving the OSCOUT input pin unconnected (open) as shown in Figure 4b.



NOTE A: The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 4. Recommended Crystal/Clock Connection

clock divider module (CDM) specifications

timing requirements for CDM circuits enabled or disabled

		MIN	MAX	UNIT
$f_{(OSC)}$	Input clock frequency	4	20	MHz
$t_{c(OSC)}$	Cycle time, OSCIN	50		ns
$t_{w(OSCIL)}$	Pulse duration, OSCIN low	15		ns
$t_{w(OSCIH)}$	Pulse duration, OSCIN high	15		ns
$f_{(OSCRST)}$	OSC FAIL frequency†		53	kHz

† Causes a device reset (specifically a clock reset) by setting the RST OSC FAIL (GLBCTRL.15) and the OSC FAIL flag (GLBSTAT.1) bits equal to 1. For more detailed information on these bits and device resets, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

switching characteristics over recommended operating conditions for clocks‡§¶

PARAMETER		MIN	MAX	UNIT
$f_{(SYS)}$	System clock frequency		20	MHz
$f_{(ICLK)}$	Interface clock frequency		20	MHz
$f_{(ECLK)}$	External clock output frequency for ECP Module		20	MHz
$t_{c(SYS)}$	Cycle time, system clock	50		ns
$t_{c(ICLK)}$	Cycle time, interface clock	50		ns
$t_{c(ECLK)}$	Cycle time, ECP module external clock output	50		ns

‡ $f_{(SYS)} = f_{(OSC)} / R$, where R = {1,2,3,4,5,6,7,8}.

§ $f_{(ICLK)} = f_{(SYS)} / X$, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0.[4:1] bits in the SYS module.

¶ $f_{(ECLK)} = f_{(ICLK)} / N$, where N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL.[7:0] register bits in the ECP module.

clock divider module (CDM) specifications (continued)

switching characteristics over recommended operating conditions for external clocks (see Figure 5 and Figure 6)†‡§

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
1	$t_{w(COL)}$	Pulse duration, CLKOUT low	SYSCLK or MCLK¶	$0.5t_{c(SYS)} - t_f$		ns
			ICLK, X is even or 1#	$0.5t_{c(ICLK)} - t_f$		
			ICLK, X is odd and not 1#	$0.5t_{c(ICLK)} + 0.5t_{c(SYS)} - t_f$		
2	$t_{w(COH)}$	Pulse duration, CLKOUT high	SYSCLK or MCLK¶	$0.5t_{c(SYS)} - t_r$		ns
			ICLK, X is even or 1#	$0.5t_{c(ICLK)} - t_r$		
			ICLK, X is odd and not 1#	$0.5t_{c(ICLK)} - 0.5t_{c(SYS)} - t_r$		
3	$t_{w(EOL)}$	Pulse duration, ECLK low	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_f$		ns
			N is odd and X is odd and not 1	$0.5t_{c(ECLK)} + 0.5t_{c(SYS)} - t_f$		
4	$t_{w(EOH)}$	Pulse duration, ECLK high	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_r$		ns
			N is odd and X is odd and not 1	$0.5t_{c(ECLK)} - 0.5t_{c(SYS)} - t_r$		

† X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0.[4:1] bits in the SYS module.
‡ N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL.[7:0] register bits in the ECP module.
§ CLKOUT/ECLK pulse durations (low/high) are a function of the OSCIN pulse durations.
¶ Clock source bits selected as either SYSCLK (CLKCNTL.[6:5] = 11 binary) or MCLK (CLKCNTL.[6:5] = 10 binary).
# Clock source bits selected as ICLK (CLKCNTL.[6:5] = 01 binary).

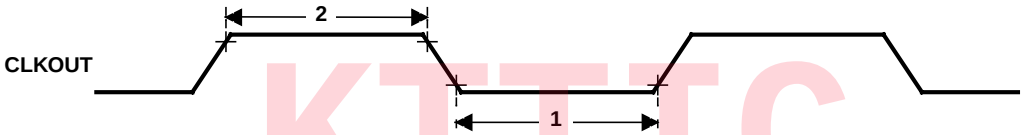


Figure 5. CLKOUT Timing Diagram

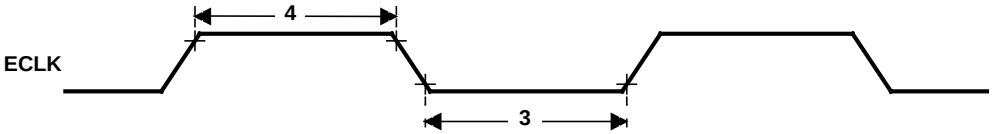


Figure 6. ECLK Timing Diagram

$\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ timings

timing requirements for $\overline{\text{PORRST}}$ (see Figure 7)

NO.			MIN	MAX	UNIT
	V_{CCPORL}	V_{CC} low supply level when $\overline{\text{PORRST}}$ must be active during power up		0.6	V
	V_{CCPORH}	V_{CC} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	1.5		V
	$V_{CCIOPORL}$	V_{CCIO} low supply level when $\overline{\text{PORRST}}$ must be active during power up		1.1	V
	V_{IL}	Low-level input voltage after $V_{CCIO} > V_{CCIOPORH}$		0.2 V_{CC}	V
	$V_{IL(PORRST)}$	Low-level input voltage of $\overline{\text{PORRST}}$ before $V_{CCIO} > V_{CCIOPORL}$		0.5	V
3	$t_{su(PORRST)r}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIO} > V_{CCIOPORL}$ during power up	0		ms
5	$t_{su(VCCIO)r}$	Setup time, $V_{CCIO} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$	0		ms
6	$t_{h(PORRST)r}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCPORH}$	1		ms
7	$t_{su(PORRST)f}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCPORH}$ during power down	8		µs
8	$t_{h(PORRST)rio}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)d}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} < V_{CCPORL}$	0		ms
10	$t_{su(PORRST)fio}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCIOPORH}$ during power down	0		ns
11	$t_{su(VCCIO)f}$	Setup time, $V_{CC} < V_{CCPORE}$ before $V_{CCIO} < V_{CCIOPORL}$	0		ns

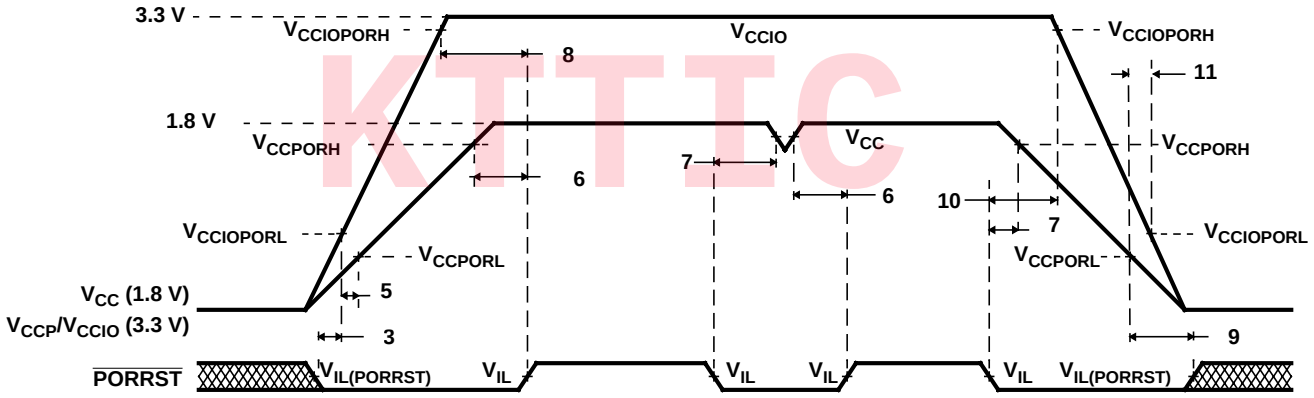


Figure 7. $\overline{\text{PORRST}}$ Timing Diagram

switching characteristics over recommended operating conditions for $\overline{\text{RST}}$†

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive	$4112t_{c(OSC)}$		ns
	Valid time, $\overline{\text{RST}}$ active (all others)	$8t_{c(SYS)}$		

† Specified values do NOT include rise/fall times. For rise and fall timings, see the switching characteristics for output timings versus load capacitance table.

JTAG scan interface timing (JTAG clock specification 10-MHz and 50-pF load on TDO output)

		MIN	MAX	UNIT
$t_{c(JTAG)}$	Cycle time, JTAG low and high period	50		ns
$t_{su(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	15		ns
$t_{h(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	15		ns
$t_{h(TCKr -TDO)}$	Hold time, TDO after TCKr	10		ns
$t_{h(TCKf -TDO)}$	Hold time, TDO valid after TCK fall (TCKf)		45	ns

input and output timings

switching characteristics for output timings versus load capacitance (C_L) (see Figure 8)

PARAMETER			MIN	MAX	UNIT
t_r	Rise time, CLKOUT, AWD, TDO	C_L = 15 pF	0.5	2.5	ns
		C_L = 50 pF	1.5	5	
		C_L = 100 pF	3	9	
		C_L = 150 pF	4.5	12.5	
t_f	Fall time, CLKOUT, AWD, TDO	C_L = 15 pF	0.5	2.5	ns
		C_L = 50 pF	1.5	5	
		C_L = 100 pF	3	9	
		C_L = 150 pF	4.5	12.5	
t_f	Fall time, $\overline{RST}$	C_L = 15 pF	2.5	8	ns
		C_L= 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_r	Rise time, all other output pins	C_L = 15 pF	2.5	10	ns
		C_L = 50 pF	6.0	25	
		C_L = 100 pF	12	45	
		C_L = 150 pF	18	65	
t_f	Fall time, all other output pins	C_L = 15 pF	3	10	ns
		C_L = 50 pF	8.5	25	
		C_L = 100 pF	16	45	
		C_L = 150 pF	23	65	

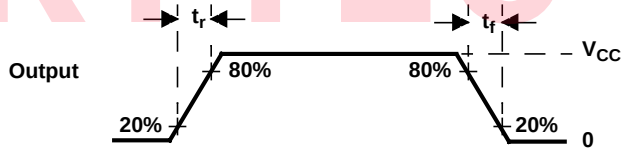


Figure 8. CMOS-Level Outputs

timing requirements for input timings† (see Figure 9)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(ICLK)}$ + 10		ns

† $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

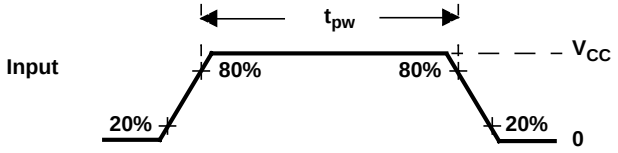


Figure 9. CMOS-Level Inputs

SPIn master mode timing parameters

SPIn master mode external timing parameters (CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)†‡§ (see Figure 10)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK ¶	100	$256t_{c(ICLK)}$	ns
2#	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3#	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4#	$t_{d(SPCH-SIMO)M}$	Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0)		10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1)		10	
5#	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	$t_{c(SPC)M} - 5 - t_f$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	$t_{c(SPC)M} - 5 - t_r$		
6#	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 0)	12		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 1)	12		
7#	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0)	10		ns
	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1)	10		

† The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
‡ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
¶ When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn master mode timing parameters (continued)

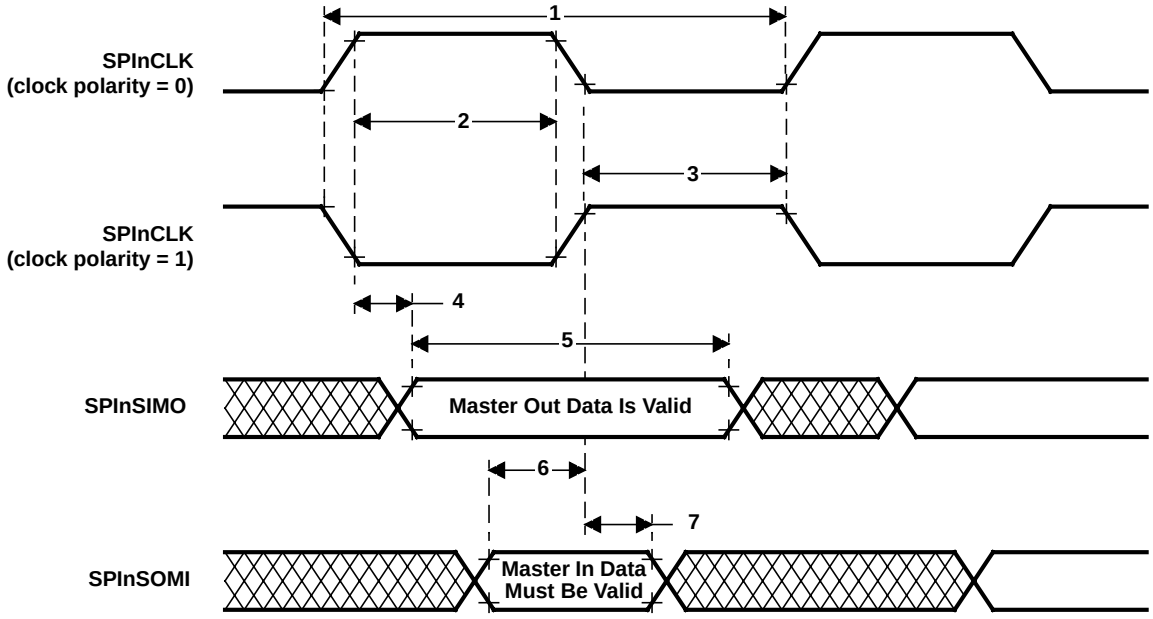


Figure 10. SPIn Master Mode External Timing (CLOCK PHASE = 0)

SPIn master mode timing parameters (continued)

SPIn master mode external timing parameters (CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)†‡§ (see Figure 11)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK ¶	100	$256t_{c(ICLK)}$	ns
2#	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3#	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4#	$t_{v(SIMO-SPCH)M}$	Valid time, SPInSIMO data valid before SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPInSIMO data valid before SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		
5#	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 5 - t_r$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 5 - t_f$		
6#	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 0)	12		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 1)	12		
7#	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	10		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	10		

† The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is set.
‡ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
¶ When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn master mode timing parameters (continued)

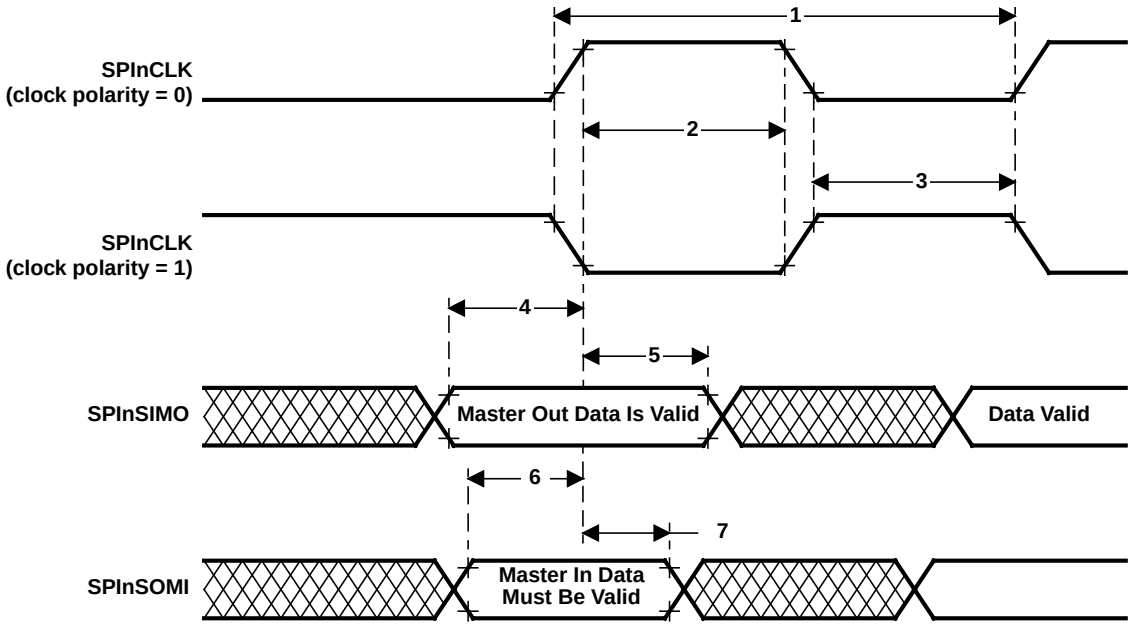


Figure 11. SPIn Master Mode External Timing (CLOCK PHASE = 1)

SPIn slave mode timing parameters

SPIn slave mode external timing parameters (CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)†‡§¶ (see Figure 12)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK#	100	$256t_{c(ICLK)}$	ns
2‖	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3‖	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4‖	$t_{d(SPCH-SOMI)S}$	Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0)		$12 + t_r$	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1)		$12 + t_f$	
5‖	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity =0)	$t_{c(SPC)S} - 12 - t_r$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity =1)	$t_{c(SPC)S} - 12 - t_f$		
6‖	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 0)	10		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 1)	10		
7‖	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	10		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	10		

† The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
‡ If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1.[12:5].
§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
¶ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
# When the SPIn is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
‖ The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn slave mode timing parameters (continued)

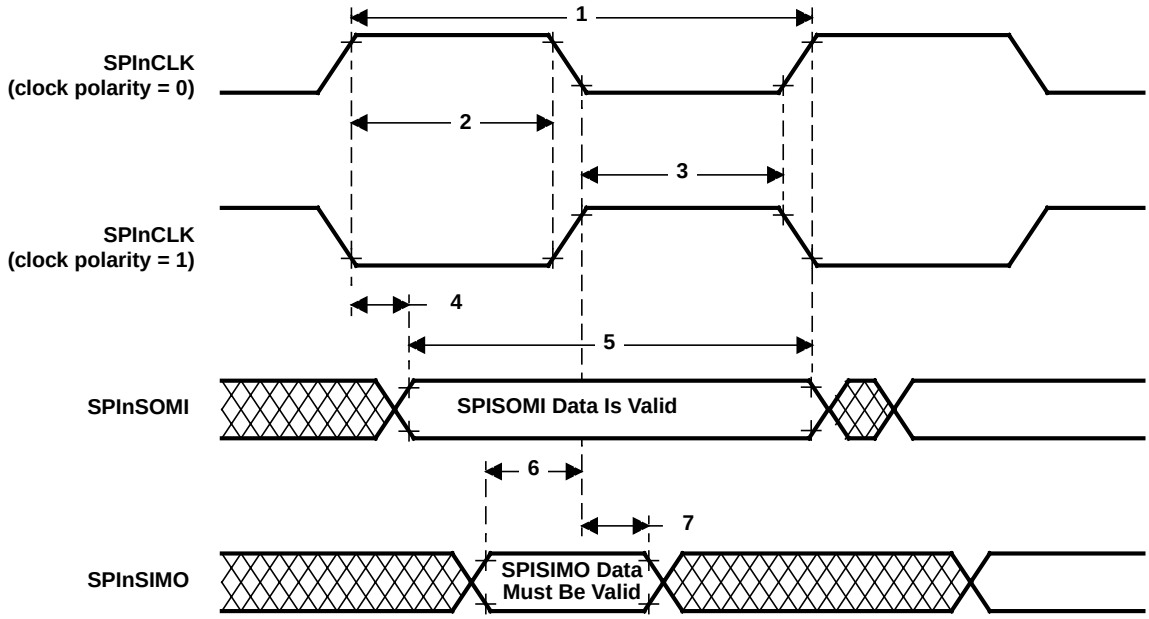


Figure 12. SPIn Slave Mode External Timing (CLOCK PHASE = 0)

SPIn slave mode timing parameters (continued)

SPIn slave mode external timing parameters (CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)†‡§¶ (see Figure 13)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK#	100	$256t_{c(ICLK)}$	ns
2‖	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
3‖	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
4‖	$t_{v(SOMI-SPCH)S}$	Valid time, SPInSOMI data valid before SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-12-t_r$		ns
	$t_{v(SOMI-SPCL)S}$	Valid time, SPInSOMI data valid before SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-12-t_f$		
5‖	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity =0)	$0.5t_{c(SPC)S}-12-t_r$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity =1)	$0.5t_{c(SPC)S}-12-t_f$		
6‖	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 0)	10		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 1)	10		
7‖	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	10		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	10		

† The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is set.
‡ If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1.[12:5].
§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
¶ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
# When the SPIn is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
‖ The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn slave mode timing parameters (continued)

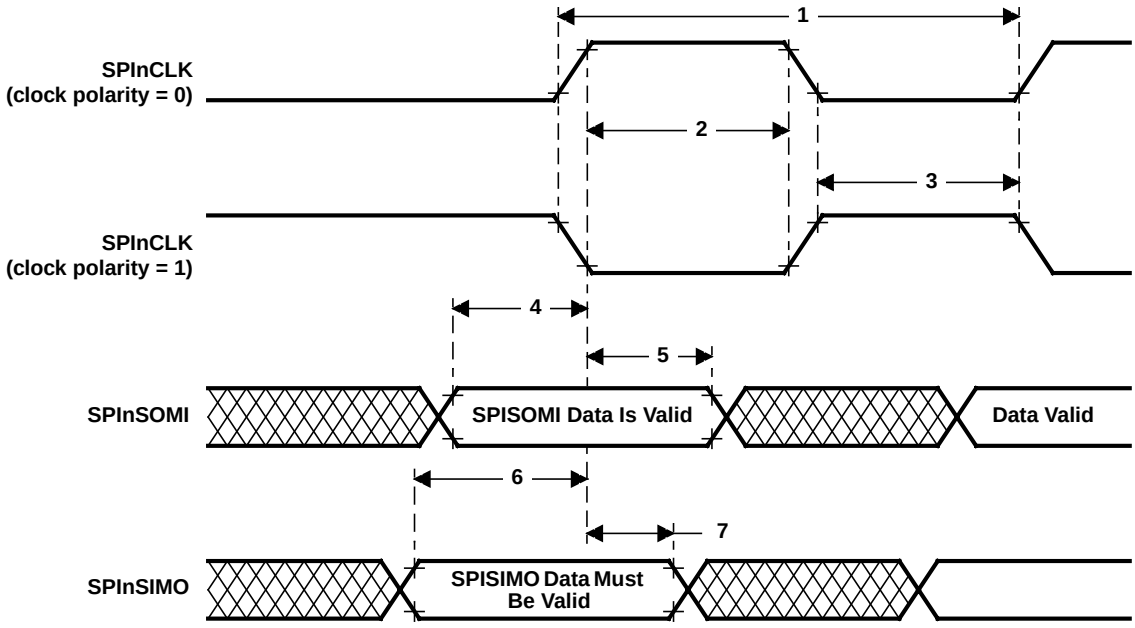
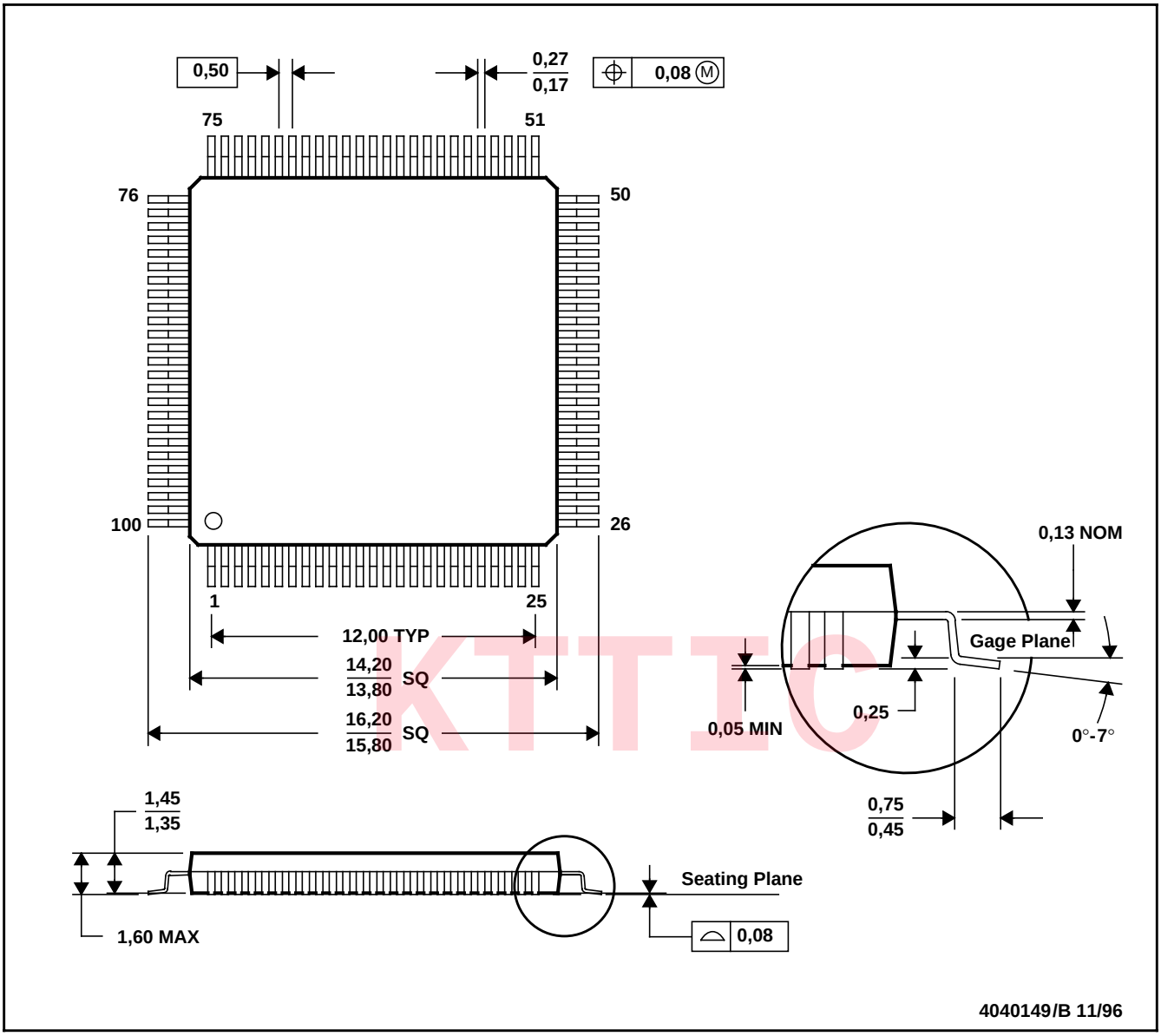


Figure 13. SPIn Slave Mode External Timing (CLOCK PHASE = 1)

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	51
$R_{\Theta JC}$	5

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REVISION HISTORY

REV	DATE	AUTHOR	NOTES
B	10/02	R. Haley	Updates:' Page 8, Pull-down added to $\overline{\text{TRST}}$ and CLKOUT pins Page 20, V_{CC} min changed to 1.71 V Page 21, V_{CC} changed to 2.05 V in I_{CC} test conditions Page 21, I_{CCIO} Standby changed to 100µA
A	9/02	R. Haley	Typographical Changes: Page 25 and 26, V_{CC} corrected to V_{CCIO} in table note Updates: Throughout,Names of Reference Guides updated Throughout, 1.4mm thickness plastic quad flatpacks referred to as LQFP Page 8, Option to leave TEST pin disconnected removed from description Page 15 and 16, development system support updated Page 20, V_{CC} max changed to 2.05 V, nom value deleted Page 21, V_{CC} changed to 2.05 V throughout table Page 21, note concerning V_{IL} value for the $\overline{\text{PORRST}}$ pin added
*	11/01	R. Haley	Initial version

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